Nanochannel fabrication and characterization using bond micromachining

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1

Introduction

This chapter will give an introduction into nanochannels and technologies to fabricate them. The need for developing new technologies to create nanochannels will be explained. Also, the general outline of the rest of this thesis will be discussed.

1.1 Nanochannels

The title of this thesis, “Nanochannel fabrication and characterization using bond micromachining”, refers to the need for developing new technologies to enable us to create smaller and smaller (fluidic) channels.

In recent years, the fabrication of nanometer-sized channels and tubes has gained considerable attention because of their potential use in chemical and DNA analysis and synthesis devices [1, 2], in nanofluidic pumps [3], or as key components in very sensitive chemical sensors [4, 5]. Nanochannels can also be used for electrophoresis [6-8] or electro-osmotic flow systems [9-11]. Furthermore, they are considered very important for studies involving single molecule dynamics and fundamental research concerning the properties of fluids in these kinds of confinements.

In essence, nanochannels can be divided into two categories. One-dimensional (1D) nanochannels are defined as channels having one of the dimensions (usually the depth) in the sub-micrometer range. Similarly, 2D nanochannels are channels which have both the width and the height in the nanometer range. An artist impression of a 1D nanochannel (with fluidic access tubing) can be found in Figure 1-1.

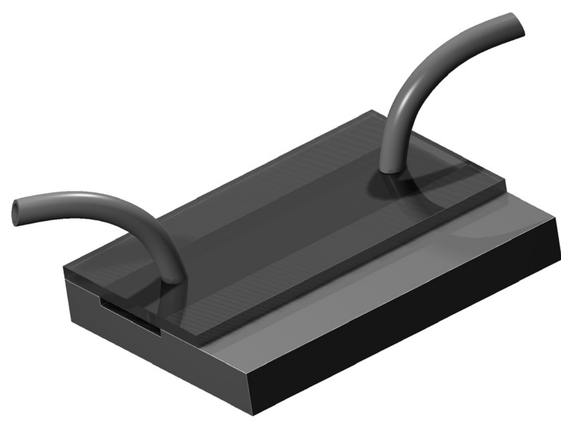

Figure 1-1: *Artistic impression of a 1D fluidic nanochannel.*

A lot of the applications make use of the characteristic features of nanochannels. Some of the main characteristics that separate them from microchannels are:

- Large surface-volume ratio (thus a large interaction between the fluid and the channel wall).
- Electric double layer effects (see chapter 4).
- Size-effects of molecules and ions in nano-confinement (e.g.: will there be changes in the viscosity of the fluid as the channel dimensions approach the molecular dimensions?).

1.2 Micromachining technology as a tool for nanochannel fabrication

Micromachining is the term used to describe the fabrication of structures with micrometer-sized features, generally using silicon as a substrate material. These structures, used as sensors, actuators or fluidic systems, are often called MEMS (Micro Electro Mechanical Systems). Micromachining is based on IC technology processes: film deposition, lithography and film etching, together with additional technologies to create three-dimensional structures. Microsystems can be designed and fabricated for a wide variety of applications, for instance accelerometers in airbag systems [12-14], mechanical micro grippers [15-17], micro total analysis systems [18-20], and data storage systems [21-23]. As the race for creating smaller and smaller structures continues, a new field emerges in the form of nanotechnology, which can be described as the area of science and technology where dimensions in the range of 100 nm or smaller play a critical role. It is a multidisciplinary area of research, combining biology, materials engineering, physics, electrical and mechanical engineering to create nanosystems for information storage, single molecule detection, fuel cells, etc. In a lot of these systems, nanofluidic channels are a key element.

Often, the tools used in micromachining can be used in nanosystem fabrication. For overviews of silicon micro- and nanomachining technology, see [24-27]. The two main categories into which silicon machining technology can be divided are bulk machining and surface machining. Bulk machining is essentially the processing of the actual silicon bulk wafer, usually by means of dry (plasma) etching or wet anisotropic etching in basic solutions such as potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH). Surface machining usually uses a stack of thin (100 nm-10 μm) layers which are deposited onto the silicon substrate, and then machined (by lithography, plasma etching and wet etching techniques) to

define and, if necessary, release the free standing or moveable structure. In this approach, the silicon is essentially only used to support the finished structures. For an interpretation of the difference between bulk and surface machining: see Figure 1-2. A more detailed description of the typical steps involved in both approaches will be given in the next paragraphs. In addition, bond micromachining will be discussed: a technique in which wafer bonding is used to create e.g. nanochannels.

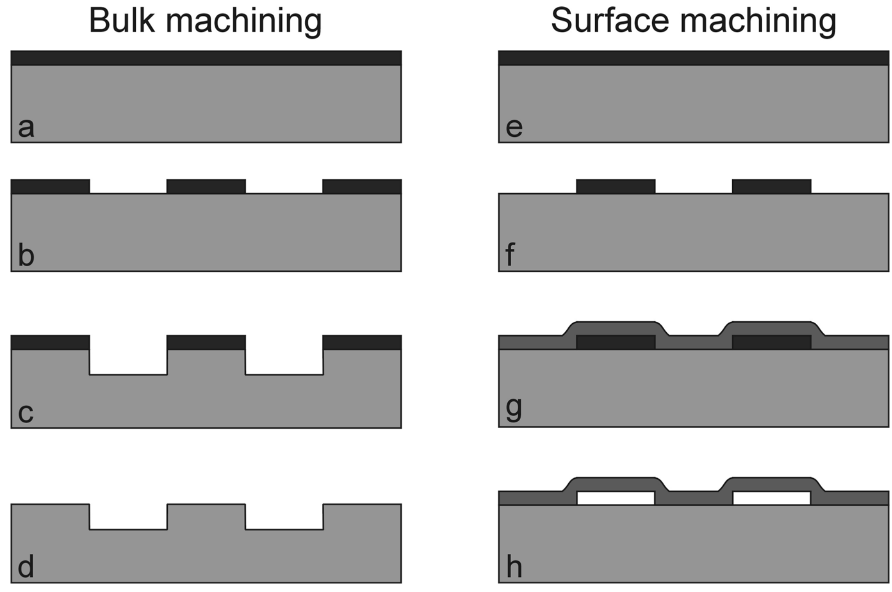

Figure 1-2: *Basic principles of bulk micromachining (left) and surface micromachining (right).*

1.2.1 Bulk micromachining

In bulk micromachining (see Figure 1-2(a-d)), generally a mask layer (for instance silicon dioxide (SiO_2), silicon nitride (SiN_x), or photoresist) is deposited on a silicon substrate (a). This layer is patterned using photolithography and wet etching or dry plasma etching (b), after which it can be used as a protective layer while etching the bulk silicon (again using wet or dry etching): (c). After the silicon etching step etching the mask can (if necessary) be removed (d) and the wafer is ready for further processing.

The main two methods for the bulk etching of silicon are wet etching and dry plasma etching. These will be discussed now, together with some other technologies which are complementary. For a more thorough study on this subject, see [27].

Wet etching of silicon

Wet etching of single crystalline silicon is generally performed using basic solutions such as KOH or TMAH solutions. The advantage of this type of wet etching is that it is of anisotropic nature: the etchant etches the silicon relatively fast in the <100> and <110> directions, and virtually stops at <111> planes [28-30]. This means that well-defined structures can be created, taking the crystallographic orientation of the wafer and the mask design into account. Besides anisotropic wet etching, isotropic wet etching of silicon is also possible, using e.g. a $HF:HNO_3$ etchant [31, 32].
In Figure 1-3 the etch profiles in <100>, <110> and <111> silicon of a simple trench etched using KOH or TMAH can be seen (note: the etching of such a channel in <111> silicon is not trivial, as the wafer surface itself is <111>). The top row shows the orientation of an octahedron bound by <111> planes, relative to the orientation of the primary flat.

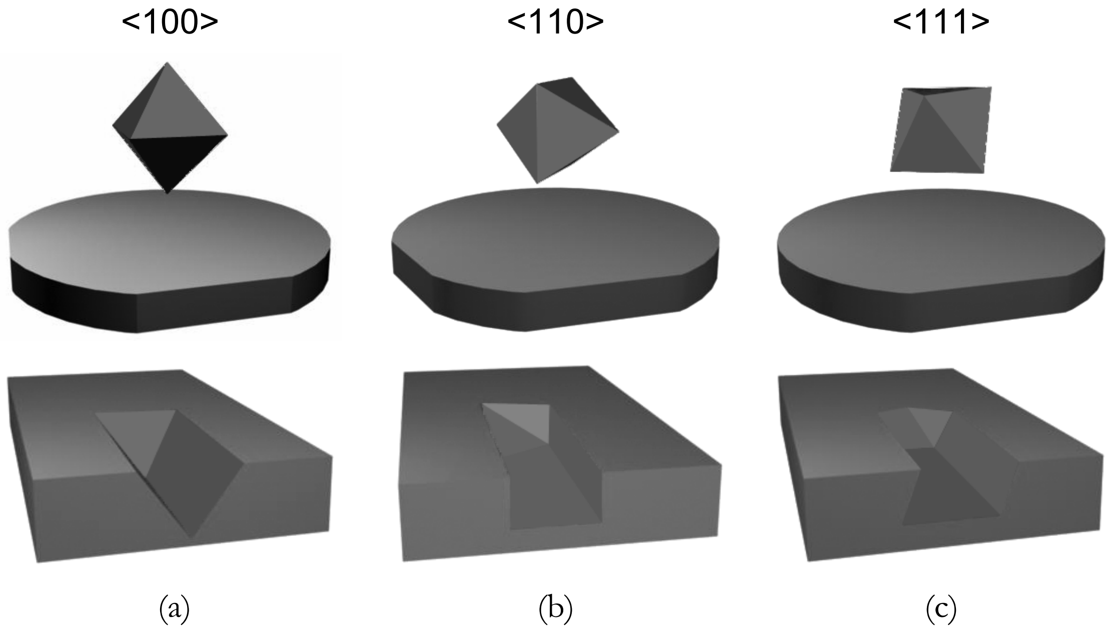

Figure 1-3: *Orientation dependent (anisotropic) wet etching profiles for (a): <100>, (b): <110>, and (c): <111> oriented silicon wafers etched in alkaline solutions. Top row: position of the octahedron limited by <111> planes relative to the wafer flat (can depend on supplier). Bottom row: cross-section of the final structure after etching a trench, aligned parallel to the primary flat of the wafer.*

If the <100> wafer was to be etched for a long period of time, the resulting structure would be a V-groove (the angle at which the <111> planes intersect the surface with an angle of 54.7 degrees). For shorter etch durations the channel

bottom is flat and the sidewalls are slanted. In contrast to this, the <110> wafer is able to provide trenches with (near-)vertical sidewalls, due to the fact that the <111> planes are positioned perpendicular to the wafer surface. The only factor limiting this is the selectivity between the etch rate of the <110> and <111> planes: this varies with the etchant used, and can be as high as 400:1 [27].

Dry etching of silicon

As an alternative to wet anisotropic silicon etching, dry plasma etching (or reactive ion etching: RIE) can be used to create structures in silicon (or films deposited on silicon) [24, 33-35]. In plasma etching, molecules are dissociated and ionized. Part of the chemically reactive species takes part in isotropic etching of the substrate, while others have a passivating function. The ions are accelerated perpendicularly to the wafer surface and physically bombard the substrate, thereby locally removing the passivation and allowing the reactive species to etch the substrate. This results in directional etching, because the passivation is only removed at the bottom of the structures (ion impact), and not at the side-walls (no ion impact). The balance between the isotropic and directional etching, together with the passivation, ultimately determines the geometry of the side-wall of the structure.

One of the advantages of RIE is that often a normal photoresist mask can be used as an etch mask, whereas in wet etching generally a dedicated mask layer (often silicon dioxide or silicon nitride) is needed, because the often very alkaline solutions effectively act as a photoresist stripping solution. There are numerous amounts of different dry etching recipes, all having different etch speeds and profiles, ranging from very anisotropic to totally isotropic [36]. The profile of the final structure depends on the process parameters used.

Other bulk etching technologies

Another way to etch bulk silicon (or glass) is powder blasting (also called sand blasting, or abrasive jet machining) [37]. This technique uses pressurized air to accelerate ceramic particles (with a size of 3 to 30 μm) towards a substrate which is masked with a patterned photosensitive rubber foil. The main advantage of this technology is the very high etch speed which can be obtained. A downside to the process is that the surface finish is rather rough after etching, and that the smallest

possible trench width which can be etched is around 10 μm. Powder blasting is routinely used to create access holes in silicon and glass wafers.
Focused ion beam milling [38] can also be used to remove bulk material. It provides very high resolution (< 50 nm), but lacks processing speed because the pattern is directly "written" into the substrate.
The same goes for laser machining [24], which has a lower resolution of 1 micrometer and is sometimes used for drilling holes in silicon wafers, and to scribe ID codes on wafers.

1.2.2 Surface micromachining

In surface machining (see Figure 1-2(e-h), [24, 39]) structures are fabricated by first depositing a sacrificial or spacer layer (or multiple layers) on a silicon substrate (e), patterning this layer (f) and then depositing a conformal capping layer (g). Then, the sacrificial layer is removed by creating access holes in the capping layer (usually by plasma etching) and subsequent etching with a wet chemical etchant, or an isotropic plasma etch step (h). One of the critical steps is this sacrificial etch step: often this step takes a substantial amount of time, because of the fact that the sacrificial layer is etched laterally (instead of perpendicular to the surface). This means that the selectivity between the sacrificial layer and its adjacent materials is a crucial factor in surface micromachining. If the selectivity is too low, excessive tapering of the channel height will occur. Other important factors are film thickness, uniformity and stress in the deposited layers. Furthermore, attention must be paid to prevent stiction of the capping layer to the substrate during release [40, 41]. Because the layers are thin and surface areas relatively large, the membranes can deflect rather easily. When the wafer is dried after wet etching of the sacrificial layer, the surface tension of the liquid pulls the structure towards the substrate, to which it can permanently adhere ("stiction"). To prevent stiction, e.g. freeze drying can be used.

1.2.3 Bond micromachining

The term bond micromachining refers to a technology to create sealed (nano)channels, using wafer bonding to seal the device. A patterned wafer with the channel structures (e.g. fabricated by bulk etching of silicon, or by surface machining of a spacer layer) is bonded to a cover wafer (usually silicon or glass), using direct bonding or anodic bonding. The cover wafer can have pre-fabricated

access holes, for fluidic connectivity. For wafer bonding very smooth surfaces are required (especially in the case of direct bonding).

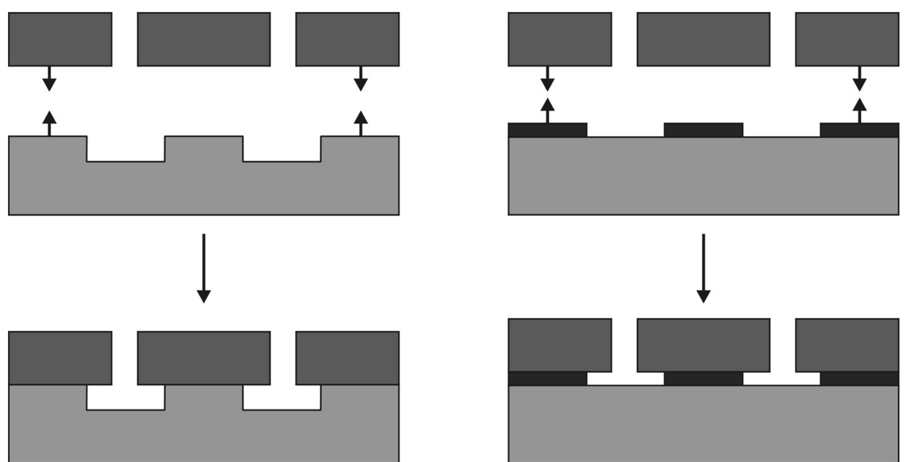

Figure 1-4: *Principle of bond micromachining. Left: based on bulk etching of silicon and wafer bonding. Right: based on surface machining and bonding.*

The main advantage of this technology, when compared to for instance sacrificial etching of channels, is the ease of fabrication (no time consuming sacrificial etch step is needed), and the uniformity of the depth of the channels which can be obtained (when using sacrificial etching the channel height is often tapered due to limited etching selectivity between the sacrificial layer and the surrounding channel wall material. Bond micromachining will be the main technique to fabricate nanochannels throughout this thesis.

1.3 Applications of nanochannels

Although it is impossible to give a complete overview of the wide range of applications in which nanochannels are or can be used, some characteristic ones are mentioned in more detail below.

Han and Craighead [2, 42] demonstrated the separation of long DNA molecules in an entropic trap array, fabricated by standard silicon micromachining technology. Deep (1.5-3 μm) trenches are interconnected by 1D nanochannels with a height ranging from 75 to 100 nm. The structures are created in two RIE steps: the first defining the nanochannels, the second creating the deeper trenches. The etched wafer is then bonded to a Pyrex cover wafer. During the separation experiments,

initially the DNA molecules are trapped in a deep region, because their radius of gyration is much larger than the height of the nanochannels. The DNA is then separated by applying a DC field, creating electrophoretic mobility differences. The molecules can slip through a nanochannel because they are able to change their confirmation. Interestingly, large DNA molecules have a higher escape probability than small ones (because they have a larger contact area with the interface between a deep region and a connecting nanochannel, they also have a higher "escape attempt frequency").
Another examples of size separation of DNA or other large molecules is given by Chou et al. [8]. In their device, consisting of a 350 nm high channel with a two-dimensional lattice of obstacles with asymmetric disposition, the Brownian motion of large molecules (e.g. DNA) is rectified, so that the molecules follow different paths through the structure, depending on their diffusion coefficient (and thus on their size). They have achieved a 6% resolution in length of DNA molecules (in the size range of 15-30 kbp) on a 100 mm wafer scale.

An example of a nanofluidic pumping device is demonstrated by Tas et al. [3]. A sacrificial layer technique is used to create a bubble pump with a "reservoir" which fills by capillary forces, after which the liquid is forced out by applying air pressure. After ejection of the liquid, the air pressure is dropped, and the device fills by capillary force again. Reproducible dispensing of droplets of 40 pL of water has been achieved using this type of device.

Karlsson et al. [43, 44] used confocal laser induced fluorescence to detect single 30 nm-sized beads flowing through lipid nanotubes. The nanotubes have an inner diameter between 100 and 300 nm and a wall thickness of approximately 5 nm. They are drawn from the lipid bilayer of a vesicle by means of a micropipette.

1.4 Fabrication technologies for nanochannels

To give the reader an idea of which technologies are currently used to fabricate nanochannels, some typical examples are treated in this paragraph.

An example of using sacrificial materials, in this case polymers, to create nanofluidic channels, is given by Li et al. [45]. A polynorbornene (PNB) layer is spun onto a

silicon substrate, and is then patterned using standard photolithography, followed by reactive ion etching of the PNB layer. A capping layer (silicon dioxide, silicon nitride or polyimide) is conformally deposited, after which the PNB layer is removed by thermo-decomposition at a temperature of 425°C, leaving channels with a height ranging from 40 μm to 100 nm.

Eijkel et al. [46] use a somewhat similar method, although they use aluminum as a sacrificial layer to form all-polyimide 1D nanochannels. First a layer of polyimide is spin coated on a silicon substrate, then a 100 or 500 nm thick layer of aluminum is sputter deposited, and patterned using standard photolithography and wet etching of aluminum. Subsequently a second layer of polyimide is spin coated and patterned using UV exposure and development. After curing the polyimide layer, the aluminum is etched during 20 hours in aluminum etchant. Capillary filling with water, isopropanol and ethanol was demonstrated. The 500 nm deep channels all filled readily with the fluids, however for the 100 nm deep channels the filling could only be performed for channel widths up to 5 μm. Wider channels appeared to collapse during the drying process at the end of the fabrication sequence.

Foquet [1] demonstrates a sacrificial method to fabricate channels, which can later be used for DNA fragment sizing. On a fused silica substrate, a 300 nm layer of polysilicon is deposited, which is patterned to leave the intended channel structure. The whole wafer is then capped with a 1 μm thick layer of fused silica, and after creating access holes, the polysilicon sacrificial layer is removed by etching in 5% TMAH at 75°C, for a period of 4 hours. Stern et al. have developed a similar technology to fabricate nanochannels for chemical sensors [4], using a 20-100 nm thick layer of amorphous silicon as the sacrificial layer, and stoichiometric silicon nitride (Si_3N_4) as the capping layer.

Recently, Kutchoukov et al. [47] have used reactive ion etching of glass to create 1D nanochannels in Borofloat glass wafers: a 33 nm thick amorphous silicon layer is patterned and used as a RIE mask to etch channels in the glass wafer. The channel depth is defined by the etching time, and consists of the thickness of the amorphous silicon layer, plus the glass etch depth. After etching the wafers are bonded anodically.

The same principle has been used by Kameoka and Craighead [5] to fabricate a refractive index sensor using photon tunneling in a nanofluidic channel.
Mao et. al. [48] fabricated planar nanofluidic channels (similar to Figure 1-1) using reactive ion etching of silicon and anodic bonding to a glass wafer, or by wet etching of Pyrex or Borofloat glass using buffered oxide etchant, and subsequent direct bonding to another glass wafer. The authors report channel collapse when using anodic bonding in combination with low channel depth and high channel width (20 nm × 10 μm, 40 nm × 20 μm).

A demonstration of the fabrication of self-sealing, flexible, polymer nanochannels is given by Ilic et al. [6]. First a silicon mold is fabricated, containing trenches with a width between 400 nm and 20 μm, and a height ranging from 2 to 20 μm. Then, vapor deposition of parylene is used to seal the channels. The non-conformal step coverage associated with his deposition process forms flexible parylene nanotubes inside the trenches, with an inner diameter in the 100 nm regime. Capillary and electrophoretic driven flow was demonstrated in capillaries up to 5 cm in length. A drawback of this technique is that it is difficult to gain complete control over the inner dimensions of the resulting nanotubes.

Another method to create nanochannels (in this particular case two-dimensional) is fast atom beam etching, employed by Hibara [49]. Nanochannel patterns were defined in a resist layer using E-beam lithography. The resist pattern is then transferred to the underlying silicon substrate in an atom beam etcher. In this machine CHF_3 gas is first ionized, then accelerated by a high voltage, and finally neutralized, before hitting the substrate with atom velocities around 100 km/s. This way, 330 nm and 850 nm sized channels were fabricated. The authors also performed filling of the channels with water and fluorescent solutions. A noticeable filling speed reduction was observed in the 330 nm sized channels (the mean velocity was four times slower than expected).

1.5 Aim of this thesis

The continuously growing interest in artificial nanostructures has stimulated the search for novel nanofabrication techniques. All mentioned techniques to construct nanochannels have some drawbacks. The surface nanomachining method is rather

complex and, unless special access holes are used, long etch times are needed to remove the sacrificial layer completely. In this case the selectivity between sacrificial and capping layer is also of importance, because it will ultimately determine the amount of tapering in the channel height. The mentioned bulk and bond machining techniques usually make use of expensive RIE equipment and special masks for pattern transfer. RIE normally creates rough surfaces and the sidewalls of the trench can be tapered. Especially when the width of the trench is in the same order of magnitude as the trench depth (i.e. sub-100 nm), the roughness and shape of the sidewalls will have a major influence on the flow characteristics of the nanochannel.

This thesis will primarily deal with the development of simple and robust, yet highly accurate processes for the fabrication of 1D fluidic nanochannels. Key aspects are reducing the channel depth (below 100 nm), while keeping accurate control over it, and smooth surface finish (the channel walls, top and bottom surfaces should have very low roughness). Furthermore characterization methods (channel depth measurement) have to be addressed. Finally, ease of fabrication is an important factor: eliminating the use of expensive RIE equipment and complex and time-consuming sacrificial etch methods can cut costs and time. A step further will also be taken into the area of two-dimensional nanochannel fabrication.
Not only fabrication technology will be discussed, but also the filling behavior of fluids in nanochannels has to be studied and compared to a theoretical model.

1.6 Thesis outline

The second chapter deals with the development of a basic process flow for the creation of 1D fluidic nanochannels. Two possible approaches are discussed: anisotropic wet etching of bulk silicon and subsequent bonding, and the surface machining method of depositing and selectively etching of a spacer layer, followed by bonding. The various characteristics, advantages and limitations of both processes will be discussed, leaving us with a nanochannel fabrication “toolbox”.
In the third chapter, the creation of nanofluidic chips, with interfacing to the environment will be treated. This will involve nanochannel fabrication, as described in chapter two, but also the creation of microfluidic reservoirs, measurement rulers on the chip, and bonding of the silicon wafers to Borofloat glass wafers, which have pre-fabricated access holes to enable fluid injection.

After the fabrication of complete chips, they are analyzed in chapter four: various liquids will be introduced into the chips by means of capillary filling. A model for the filling speed will be developed, based on the classical Washburn theory, and the actual filling speed of the channels will be determined using optical microscopy, in combination with a digital video camera. The theoretical and experimental values for the filling speed will be compared.

Taking nanochannel fabrication one step further, in chapter five some first steps are taken to fabricate two dimensional nanochannels. Two possible ways are suggested. The first is via the use of local oxidation of silicon (an edge lithography method), in combination with nano imprint lithography. The second one is by directly creating channels with sub-micrometer width and depth by using laser interference lithography in combination with wet anisotropic etching of silicon, using the same process as in chapter three.

Finally, chapter six will consist of a detailed overview of the main conclusions of this thesis and recommendations for future research.

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2

Fabrication of 1D nanochannels[*]

This chapter deals with the issues concerning the fabrication of 1D fluidic nanochannels. Two possible technologies are described and developed: one where the channels are etched using wet anisotropic etching of <110> silicon wafers (bulk machining), and one where the channel is formed by selectively etching of a well defined oxide layer (surface machining). Both methodologies have their own characteristics, advantages and disadvantages, which will be discussed.

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[*] In this chapter, the paragraphs involving wet anisotropic etching of <110> silicon are based on: J. Haneveld, H. Jansen, E. Berenschot, N. Tas, and M. Elwenspoek, "Wet anisotropic etching for fluidic 1D nanochannels," *Journal of Micromechanics and Microengineering*, vol. 13, pp. 62-66, 2003.

2.1 Wet anisotropic etching of <110> silicon for 1D fluidic nanochannels

Standard technologies to etch channels [1, 2] with nanometer depth, all suffer from one or more drawbacks. RIE, for instance, can produce channels with sub-micrometer depth in silicon [3] or in glass [4], but the exact channel depth is not easily controlled, because the etch rate is generally considerably high. Also, RIE can leave a rough surface finish and, depending on the process parameters, tapered sidewalls. To be able to etch fluidic 1D channels with a well defined and controlled geometry, a process was developed, which uses wet anisotropic etching of silicon by TMAH, in combination with <110> wafers, giving the possibility to create channels with rectangular cross-sections. This also simplifies the modeling of fluid behavior in these channels. Moreover, due to the low lateral etch rate, control over the line width is excellent. This is of importance when the width of the channels is also reduced to sub-micrometers.

2.1.1 Etchant selection

As stated before, for nanofluidic applications (using channels with a depth below 100 nm) it is important that the etch depth is well controlled and the surface roughness is minimized. The etch rate of the etchant should be low enough to allow for accurate etch depth control, but also high enough to be of practical use. To reduce roughness, the addition of additives such as surfactants is an option [5, 6]. To select the best wet etchant for creating sub-100 nm channels, 2.5% KOH, NaOH and TMAH solutions were investigated. Samples etched in aqueous KOH, NaOH and TMAH clearly showed a roughened surface after the etching process. A separate fourth sample, etched in Olin OPD 4262 developer (Arch Chemicals, containing 2.5% TMAH and a number of surfactants), had a very smooth finish after etching. The smooth surface in comparison to the samples etched in a standard 2.5% TMAH solution must be caused by the addition of the surfactants to the OPD 4262 solution. However, the addition of surfactants does not necessarily have such a big positive effect, as was proven in a test with a 5% NaOH solution versus Clariant AZ 351B NaOH developer, which also contains 5% NaOH (see Figure 2-1). The surface roughness did improve due to the additives in the

developer, but the resulting surface was still far from being as smooth as that of the samples etched in OPD 4262.

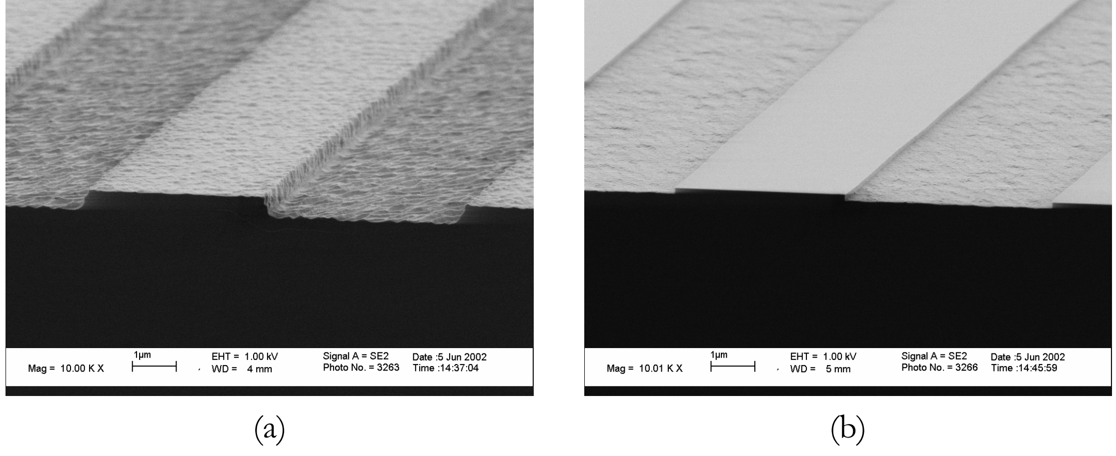


Figure 2-1: *Effect of surfactant addition to NaOH solution. (a) <110> silicon, etched for 15 minutes in a 5% NaOH solution. (b) Etched in a Clariant AZ 351B NaOH developer diluted to 5% NaOH content. Note that the surface finish improves, and that the etch rate decreases.*

An example of a <110> silicon wafer, etched in OPD 4262, can be found in Figure 2-2. The surface finish of the bottom of the trench is by far superior to all other candidates, and roughness could not be observed by high resolution scanning electron microscopy.

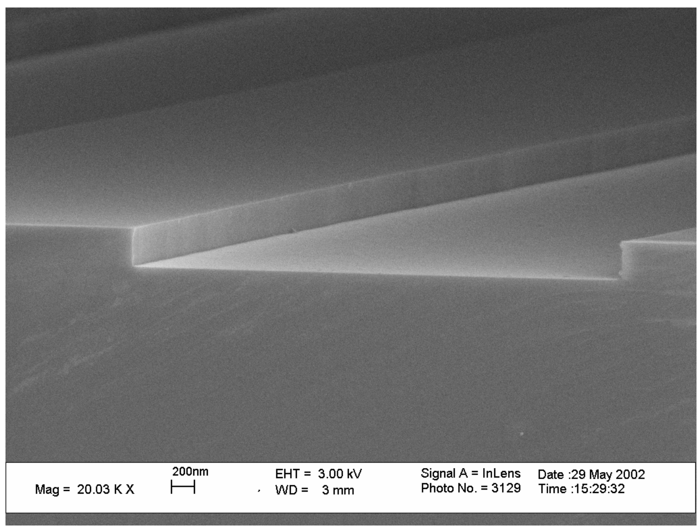


Figure 2-2: *<110> silicon etched in OPD 4262 developer. Notice the straight and vertical sidewalls, as well as the extremely smooth surface at the bottom of the trench. The step height was determined to be 335 nm.*

2.1.2 Mask material selection

Normally, when using wet bulk etching of silicon in alkaline solutions (generally KOH), a mask layer is deposited on the substrate. This is generally a layer of silicon dioxide (SiO_2) or silicon nitride (SiN_x). In the next step of the process this layer is patterned using photolithography and wet or dry etching of the mask layer. The resulting patterned mask layer is then used as an etch mask for the actual etching of the silicon wafer. For this, it is useful that the ratio of the etch rates of silicon and silicon dioxide (or nitride) is very high, as can be seen in Table 2-I. The selectivity for silicon and silicon nitride is even 30 times better.

Material	**Etch rate in 25% KOH @ 75°C**	**Selectivity towards <100>**
Si <100>	60 μm/hour	1
Si <110>	100 μm/hour	0.6
Si <111>	0.75 μm/hour	80
SiO_2 (thermal)	0.18 μm/hour	$3 \cdot 10^2$
SiN_x (silicon rich)	<0.006 μm/hour	$1 \cdot 10^4$

Table 2-I: *Etch rate comparison of silicon and mask materials in a standard KOH solution [7].*

From these values we can estimate the oxide thickness that would be necessary to etch channels with a depth up to 500 nm, using thermal oxide as a mask and 25% KOH at 75°C as the etchant. The required SiO_2 thickness is $500 \cdot 0.18/60 = 1.5$ nm. The native oxide layer, which is always present on a silicon wafer due to cleaning in HNO_3, Piranha solution or spontaneous oxidation in air, has a thickness which is normally assumed to be between 0.5 and 2 nm [8]. In our case the selectivity between silicon <110> and native oxide may be different than the one based on the values in Table 2-I, because instead of KOH we use OPD 4262 as an etchant, at room temperature. Still, the native oxide might provide a sufficiently thick mask to etch nanochannels without the need of depositing a dedicated mask first. A proposed nanochannel fabrication process, including an etch rate determination and calibration, will be discussed in the following paragraphs.

2.1.3 Basic fabrication process

The proposed basic process for creating and sealing 1D fluidic nanochannels in <110> silicon, using native oxide as a mask material, is depicted in Figure 2-3.

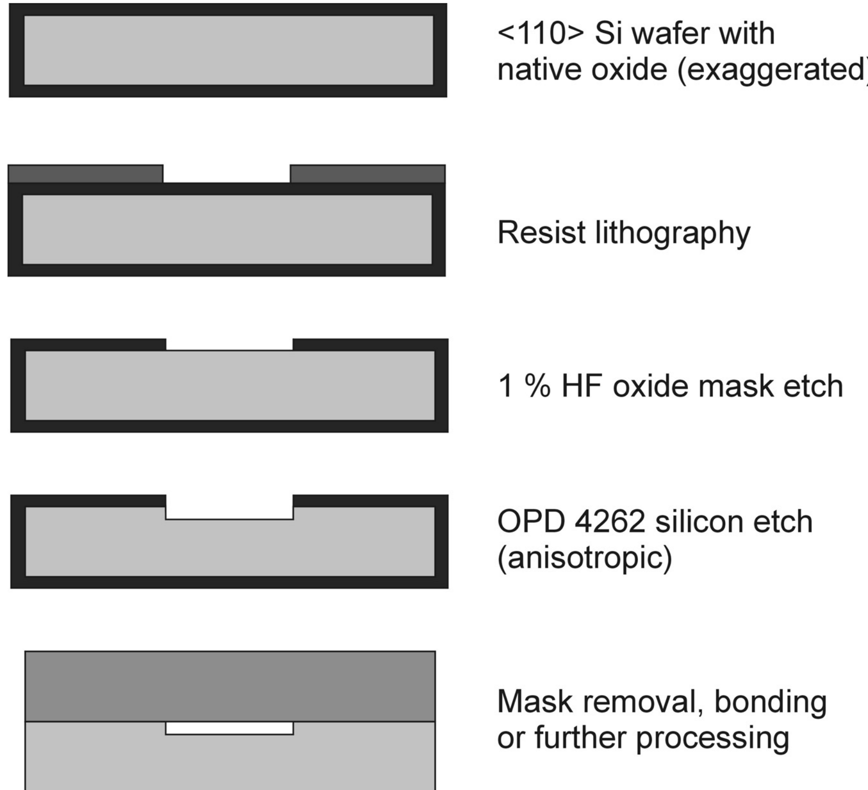


Figure 2-3: *Basic process for the fabrication of nanochannels using wet anisotropic etching of <110> silicon.*

Lithography

A <110> p-type silicon wafer is used in the experiments. Using this wafer, the following lithographic steps are performed: after a dehydration step (>10 min at 120ºC), an adhesion layer (HMDS: HexaMethylDiSilizane) and photosensitive resist (Olin 907/12) are subsequently spin-coated (20 seconds at 4000 rpm). Then, after a softbake (1 min at 95ºC), the resist is exposed (4 sec at 12 mW/cm^2) using an ElectroVisions 620 exposure apparatus (EVG), and a mask containing 4 µm wide lines and spacings. After this, a post exposure bake (1 min at 120ºC) is performed followed by development of the exposed resist by a standard 2.5% water diluted TMAH solution (Olin OPD 4262).

Pattern transfer to native oxide layer
After lithography, a 1% HF dip (1 min) is done to transfer the resist pattern to the native oxide layer. This is rather longer than the time which is necessary to remove the native oxide layer (approximately 20 seconds). The reason for this generous overetch is to be absolutely sure that all of the oxide is removed for the etching process. Then the wafer is immersed in acetone for one minute to strip the resist, directly followed by an isopropanol (IPA) cleaning dip (1 min), after which the wafer is blow-dried with nitrogen gas. The reason for the use of the IPA dip is that it removes the acetone (together with any dissolved photoresist) from the surface of the wafer before the drying. IPA also leaves a much cleaner surface than acetone when blow-drying (no streaks or spots on the wafer).

Anisotropic wet etching of silicon
The pattern transfer into the native oxide is directly followed by a silicon etch at room temperature using a fresh OPD 4262 solution as the wet chemical etchant and the native oxide as the mask material. Finally, the wafer is rinsed with DI water and spin-dried.

Channel depth measurement
After a surface scan with a mechanical profiler (Sloan Dektak II) to determine the depth of the silicon nanochannels, the wafer together with a cover wafer is ready for bonding or further processing of the wafer.

2.1.4 Etch rate calibration of silicon in OPD 4262 developer

To determine the usability of OPD 4262 as an etchant for creating 1D fluidic nanochannels, the etch rates of different silicon orientations were determined, as well as the influence of diluting the OPD 4262 solution, to be able to etch at various etch rates, depending on the desired channel depth.

Etch rate of silicon in OPD 4262
First, a calibration of the etch rate of silicon in pure OPD 4262 developer was performed to be able to predict the necessary etching time for a given channel depth. To accomplish this, the procedure of Figure 2-3 was used, with etch times up to 300 minutes. The etch rates of p-type silicon <100>, <110> and <111>

oriented wafers were determined to estimate the selectivity of the various orientations relative to each other. The channel depths were measured using a Dektak profilometer. The graph of the channel depth versus the time can be found in Figure 2-4.

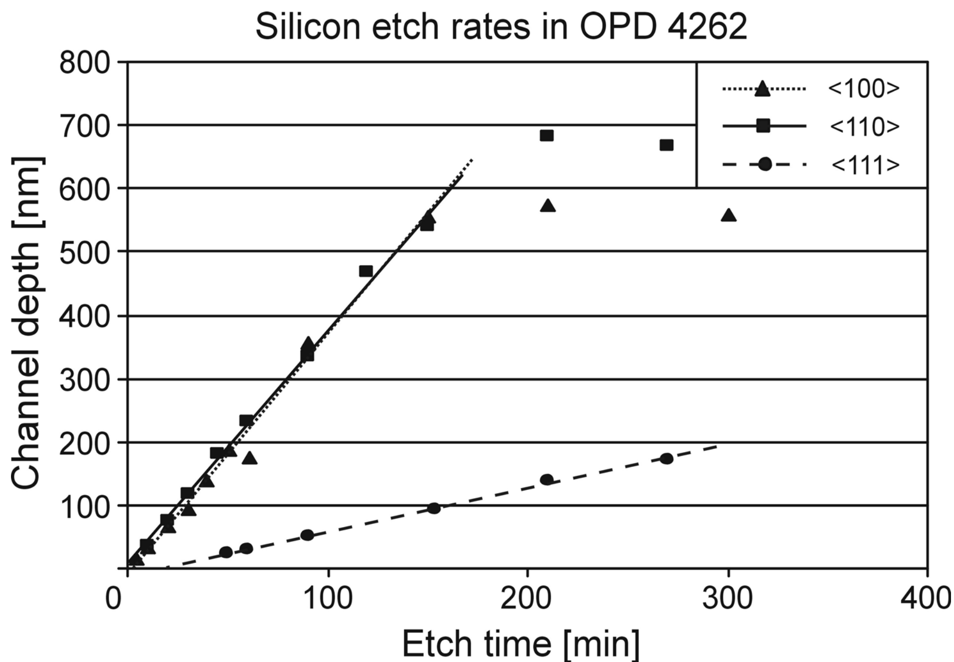


Figure 2-4: *Etch rates for silicon <100>, <110> and <111> in OPD 4262 positive resist developer at room temperature.*

From this graph some important conclusions can be drawn. The first is that OPD 4262 developer etches <110> silicon with a speed of 3.7 nm/min (220 nm/hr) at room temperature. This is a very convenient speed when aiming for nanochannels in the sub-500 nm range. The etch rates for all three silicon orientations can be found in Table 2-II.

Material	Etch rate in OPD 4262 @ room-T
Si <100>	3.8 nm/min = 230 nm/hr
Si <110>	3.7 nm/min = 220 nm/hr
Si <111>	0.8 nm/min = 50 nm/hr

Table 2-II: *Etch rate comparison of silicon <100>, <110> and <111> in OPD 4262 developer.*

Another observation is that the maximum channel depth which can be produced using this method is approximately 500 nm. At longer etching times (above 200 minutes) the channel depth does not increase any further. This is most likely due to the fact that the mask (the native oxide at the silicon surface) has worn out at this point. The fact that the etch depth stays at a more or less constant level at etching times over 200 minutes, can be explained by the fact that both the top and the bottom of the channels are now (anisotropically) etched at the same speed. Assuming an oxide thickness that can vary from 0.5 to 2 nm [8], this would give a selectivity of Si <110> over SiO_2 of at least 250:1.

Diluted OPD 4262

To try to bring down the etch rate even more, and thus to be able to create even smaller nanochannels, the effect of diluting the OPD 4262 solution was investigated. Seven different samples were etched in various concentrations of OPD 4262, ranging from pure OPD 4262 (2.5% TMAH) to pure DI water (which should not etch noticeably). The etched pattern consisted of 4 μm lines and spacings, like before. After 60 minutes of etching time, the channel depth on each of the samples was measured at three spots on the wafer. A graph of the etch depth versus TMAH concentration can be found in Figure 2-5.

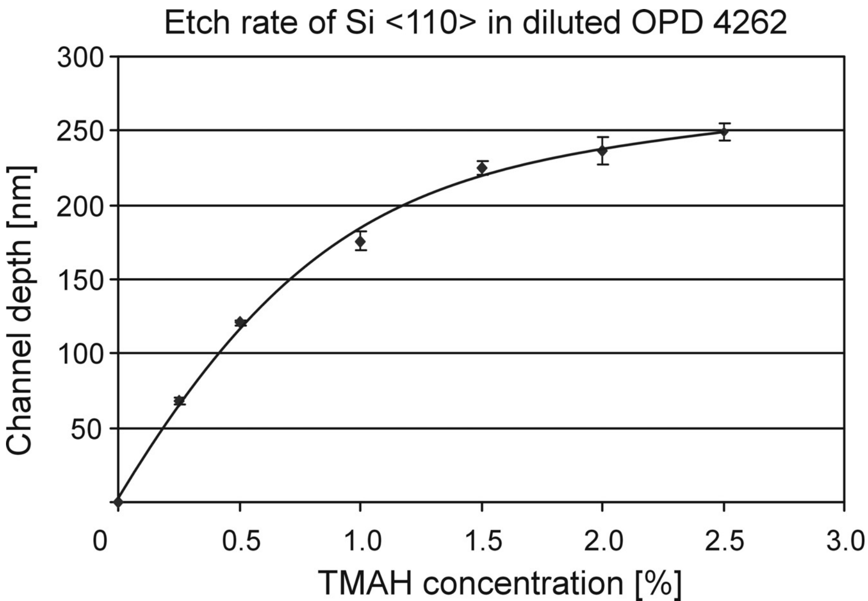


Figure 2-5: *Depth of trenches etched in silicon <110> using diluted OPD 4262 developer, after 60 minutes.*

From this graph we can conclude that a 10% OPD 4262 solution in DI water is useable when very small channel heights are desired (e.g. below 50 nm). Inspection with optical microscopy showed a smooth surface after etching.
To confirm the applicability of the 10 times diluted OPD 4262 solution for creating sub-50 nm nanochannels, a time versus etch depth measurement was also done for this particular solution. The resulting etch rate calibration can be seen in Figure 2-6.

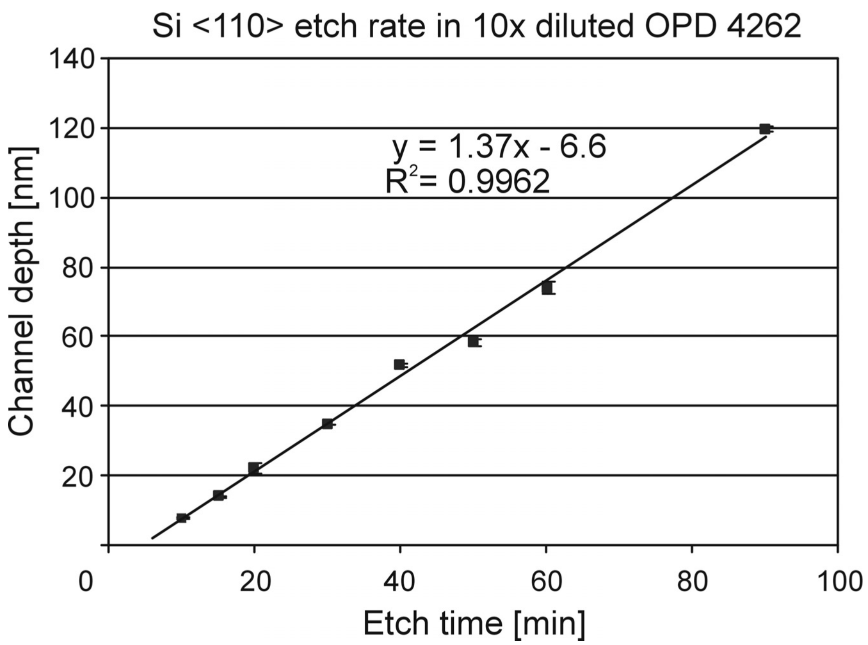


Figure 2-6: *Etch rate of silicon <110> in 10x diluted OPD 4262 developer (0.25% TMAH).*

From this graph, the etch rate of Si <110> in 10x diluted OPD 4262 can be calculated: this is 1.4 nm/min. There is a noticeable x-axis offset of approximately 5 minutes at the onset of the etching process. There are two possible explanations for the occurrence of this effect. One is that there could be a very thin layer of native oxide which is formed in the short period of time in which the wafer is exposed to air (when blow-drying the wafers after the IPA cleaning step) before the OPD 4262 etching step. In this case, also the 100% OPD 4262 solution should have an offset (of 1-2 minutes), which is very well possible, inspecting the data in Figure 2-4. Another explanation could be that the surface of the wafer is hydrogen terminated after the 1% HF etching of the native oxide. In this case, the surface has to become OH-terminated in water before the actual silicon etching can take place [9]. In any case, this offset can lead to greater non-uniformity and roughness, especially if the

etching times are small. When channels with a (well defined and predictable) depth of less than 20 nm are desired, other fabrication techniques might be preferred (e.g. by growing and selectively etching of a thin SiO_2 layer: see paragraph 2.2).

2.1.5 Direct bonding of etched wafers to silicon and Borofloat glass

Si <110> to Si <110> direct bonding procedure

Before bonding, both the etched wafer and the cover wafer undergo a 1% HF dip, a standard cleaning (10 min in fuming (100%) HNO_3, followed by 10 minutes in boiling (69%) HNO_3) and an additional Piranha cleaning to clean the silicon surfaces and to grow a well-controlled layer of native oxide on the silicon wafer surface. Then, the etched wafer is bonded to the <110> silicon cover wafer (prebond). After prebonding, the bond is annealed for 2 hours at 1100°C. This direct bonding procedure resulted in an instantaneous, near-perfect bond under an infrared camera. The high temperature needed in silicon-to-silicon fusion bonding (which can be unwanted when using certain materials in a device) can be prevented by using different bonding schemes such as anodic bonding to Pyrex wafers, or direct bonding to Borofloat wafers.

Si <110> to Borofloat glass direct bonding procedure

The etched silicon wafers are also direct-bondable with Borofloat glass wafers. Before bonding the silicon and Borofloat wafers go through a standard cleaning, and a Piranha cleaning step. After manual prebonding the bond is then strengthened by an anneal step of 4 hours at 400°C. This annealing temperature of the silicon-to-glass bond is sufficiently low to prevent plastic deformation of the glass (and thereby possibly closing of the nanochannels) and interference of the bonding process with previous micromachining steps.

The silicon-to-Borofloat bond formed an almost complete prebond by manually pressing the wafers together. After the anneal step only very few bonding defects could be observed.

2.1.6 Channel fabrication and bonding results

As an example of etched trenches, Figure 2-7 shows a channel with a step height of 335 nm. The near 90° sidewalls can be clearly seen, as well as the smooth walls and trench bottom.

Etch depth uniformity

The uniformity of the etch depth over a complete wafer was also measured and was found to be good: measuring five points across a 4” wafer showed a variation of ± 1 nm at an etch depth of approximately 50 nm (the wafers were etched for a time of 13.5 minutes). This means that the uniformity is within ± 2%.

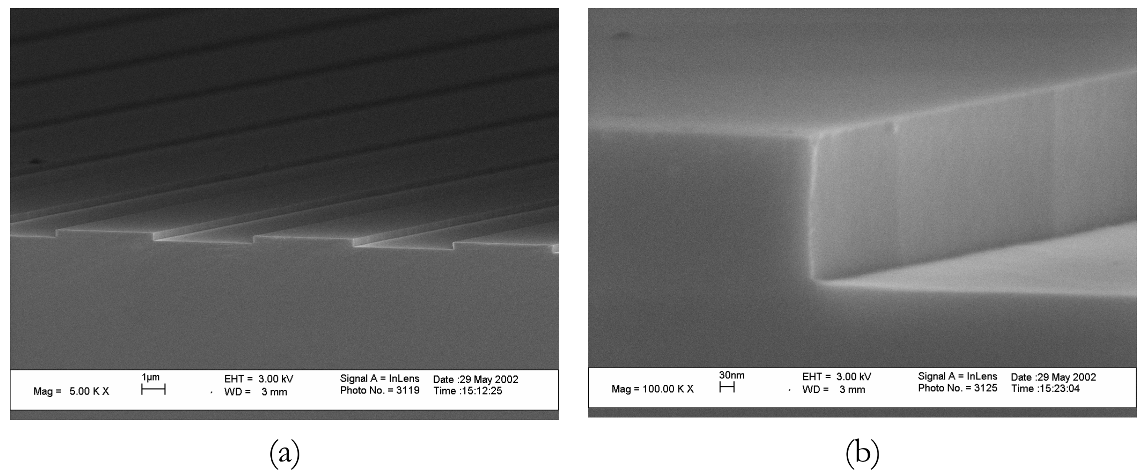


Figure 2-7: *High resolution SEM pictures of trenches with a depth of approximately 335 nm, etched in <110> silicon. (a) Overview of multiple channels. (b) Close-up.*

Surface roughness

The surface roughness on the trench bottom was measured by contact mode AFM, and was found to be approximately 0.3 nm RMS, or 0.4 nm R_a for the 335 nm deep trenches (see Figure 2-8).

Bonding results

Pictures of the cross-section of the silicon-to-silicon bond can be seen in Figure 2-9. The curved ridges on the top wafer in Figure 2-9(a) are due to the breaking of the wafer, resulting from a non-perfect alignment of the two wafers during bonding. The straight etch profile can again be seen in Figure 2-9(b). As mentioned before, the silicon wafers with trenches were also bonded to Borofloat glass wafers. Cross-sections of the resulting structures can be found in Figure 2-10.

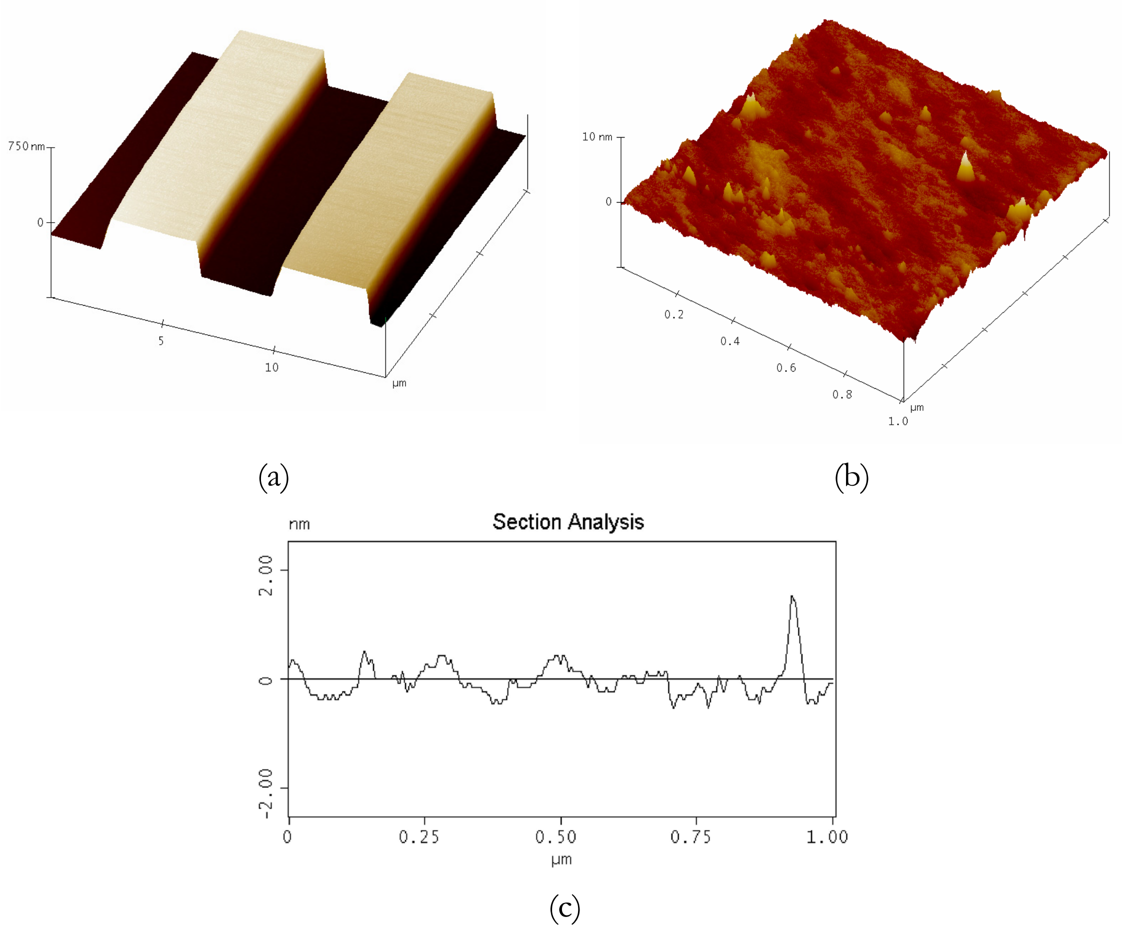


Figure 2-8: *AFM pictures of trenches with a depth of 335 nm, etched in <110> silicon. (a) 3D view. (b) Roughness measurement on the bottom of a trench. (c) Section view of (b), showing the roughness more clearly.*

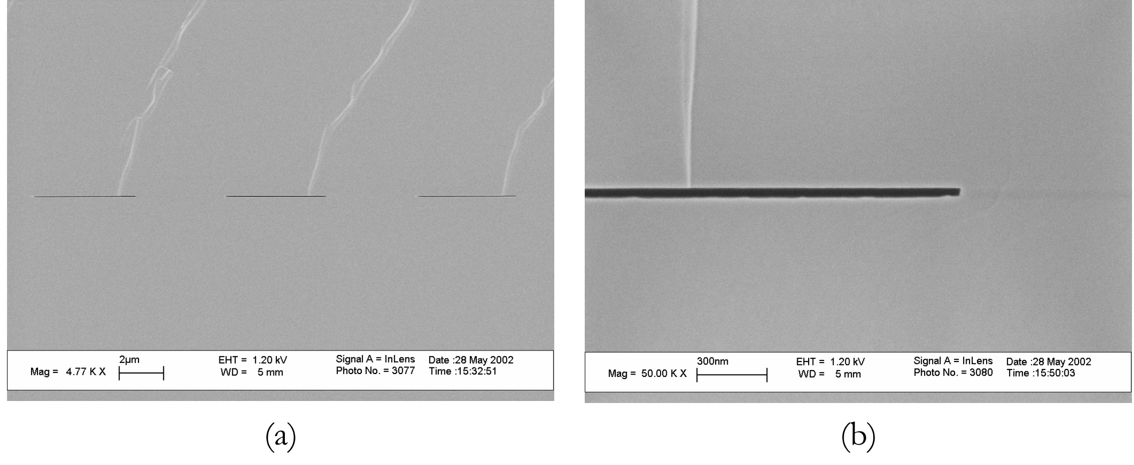
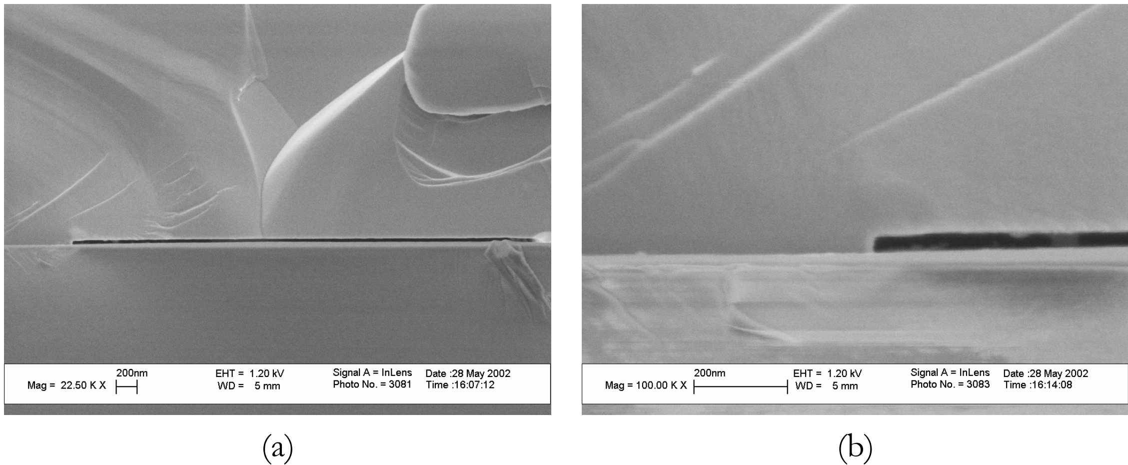


Figure 2-9: *SEM pictures of a wafer with 50 nm deep trenches, fusion bonded to a second <110> silicon wafer. (a) Cross-section of 3 channels. (b) Close-up.*



(a) (b)

Figure 2-10: *SEM pictures of a wafer with 50 nm deep trenches, fusion bonded to a Borofloat glass wafer. (a) Cross-section of one channel. (b) Close-up.*

As can be seen in the SEM pictures, the channels are completely open and no significant bending of the wafers occurs, leaving the desired rectangular cross-sectioned channels.

2.1.7 Conclusions

A simple process to anisotropically etch channels with a controlled depth up to 500 nm has been developed. Olin OPD 4262, a standard resist developer consisting of 2.5% TMAH and surfactants, is suitable as an etchant for the anisotropic etching of nanochannels with a rectangular cross-section in a silicon <110> wafer. OPD 4262 etches Si <110> at a rate of 3.7 nm/min at room temperature. If necessary, it can be diluted ten times, to obtain an etchant with an etch rate of 1.4 nm/min.

Native oxide proved to be a suitable mask material to fabricate nanochannels with a depth up to approximately 500 nm (for deeper channels, a thin thermal SiO_2 layer could be grown to act as the mask material).

The uniformity of the etch depth across a wafer was observed to be within ± 2%. Moreover, surface roughness on etched surfaces could not be observed with SEM, and contact AFM measurements indicate a roughness value below 0.5 nm, which is very low.

Furthermore, the etched wafers were successfully bonded to silicon <110> and Borofloat glass wafers to seal the channels.

2.2 Fabrication of nanochannels using a dry oxide spacer layer

As an alternative and addition to the fabrication of nanochannels by using bulk silicon machining, as described in the previous section, nanochannels can also be produced by first growing an ultrathin (5-50 nm) layer of thermal oxide, and then patterning this layer in buffered hydrofluoric acid (BHF), or dilute 1% HF. If the oxide thickness and the etching of the layer are well-controlled, this enables the very accurate production of channels with a height below 50 nm, and even below 10 nm. This would eliminate for instance the start-up effect, as observed when etching with diluted OPD 4262, which has its largest influence in this etch depth range. Another aspect is that the measurement of the channel depth can be done using very accurate optical techniques (ellipsometry), whereas the mechanical surface profilometry (used to characterize the wet etched channels from the previous paragraphs) becomes less accurate at these very small dimensions. A disadvantage of this technology is that the isotropic underetching of the mask limits the line width which can be obtained (when compared to the OPD 4262 etching method).

2.2.1 Basic fabrication process

The basic fabrication process for creating sub-50 nm 1D fluidic nanochannels, using dry oxide as a spacer layer, is depicted in Figure 2-11.

The process is largely the same as the one used for the wet anisotropic etching of silicon (Figure 2-3). The main differences here are that the <110> silicon wafer is first oxidized at a temperature of 950ºC, and no silicon etch step is included in this process (the channels are etched into the dry oxide spacer layer by means of wet etching in BHF or 1% HF: for this the resist layer undergoes a hardbake at a temperature of 120ºC, for a period of 30 minutes).

Notice that the resulting cross-section of the channels will not be rectangular; this is because of the isotropic SiO_2 etching process, using (B)HF.

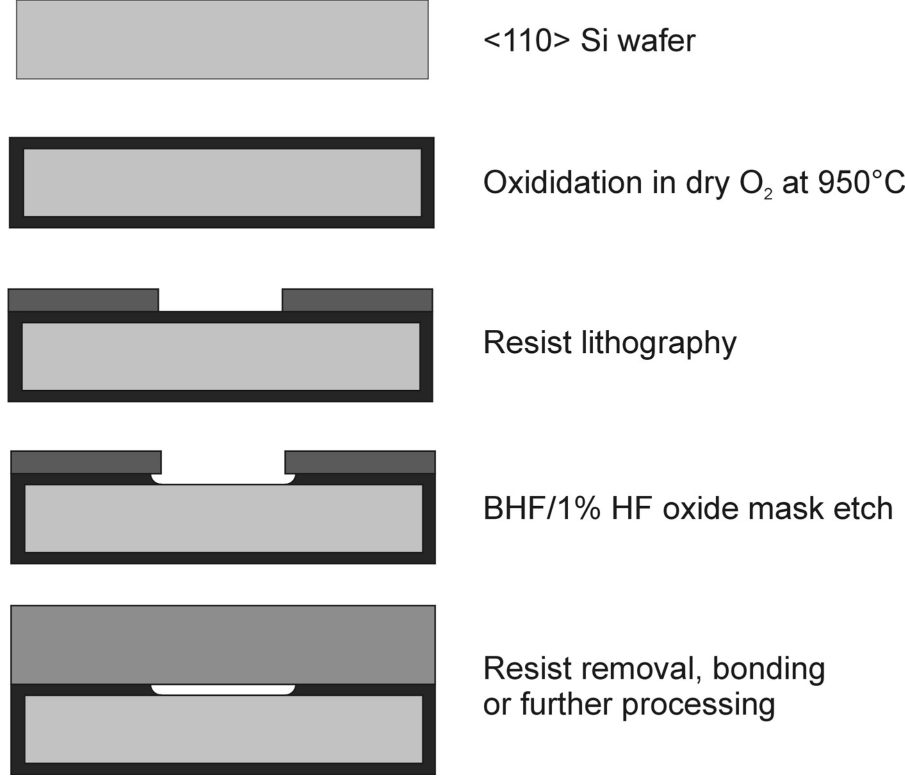


Figure 2-11: *Basic process for the fabrication of nanochannels using a dry oxide spacer layer.*

2.2.2 Dry oxidation of silicon

It is very important to have control over the thickness of the SiO_2 spacer layer, which will ultimately determine the height of the nanochannels. This layer is formed by oxidizing <110> wafers in dry oxygen at a temperature of 950ºC. The reason why dry oxidation was chosen is that dry oxide layers generally show good thickness uniformity and very smooth surface finish. The chosen temperature of 950ºC is lower than the usual 1100ºC, to reduce the SiO_2 growth rate, and thus to be able to reproducibly grow layers with a thickness of ultimately less than 10 nm. For this purpose, silicon oxidation rates in dry oxygen at 950ºC were measured: a graph of the oxide thickness versus time can be found in Figure 2-12 (for comparison, also the oxidation rate for Si <100> at 1100ºC is shown).

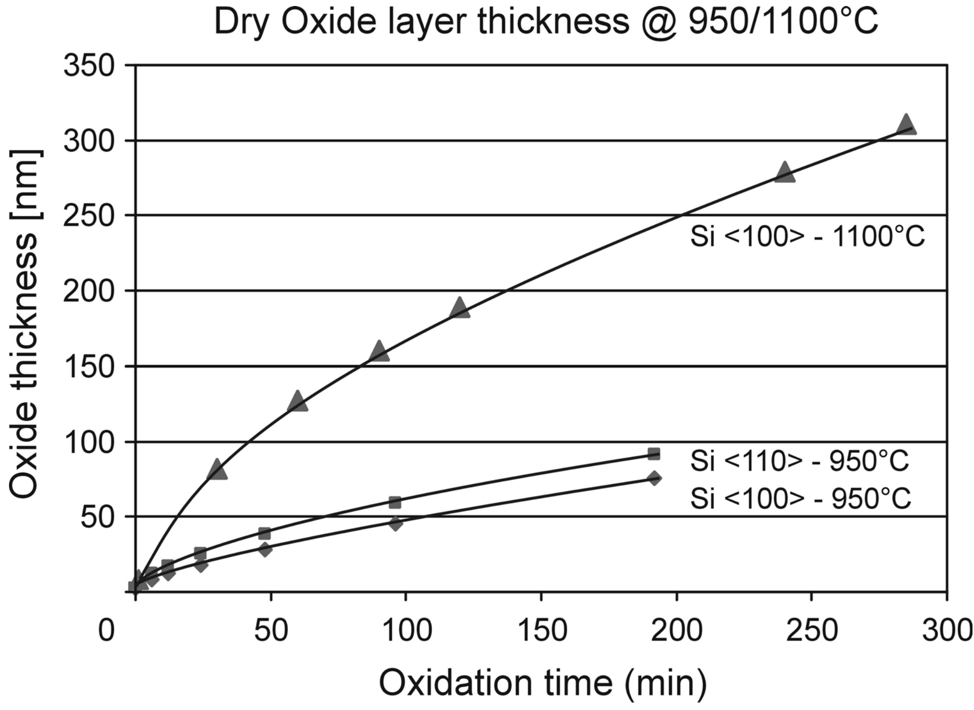


Figure 2-12: *Dry oxide thickness as a function of oxidation time at 950°C (the values for 1100°C are for comparison only, and were taken from the MESA+ clean room database).*

For our experiments silicon <110> wafers were dry oxidized at 950ºC for different durations. Following oxidation, the oxide layer thickness was measured by ellipsometry. This was done on three separate ellipsometers: a Plasmos SD 2002 ellipsometer (λ = 632.8 nm, or 1.96 eV), a multi-wavelength Woollam M-44 NIR ellipsometer (44 wavelengths ranging from 1.3 eV to 2.1 eV) and a Woollam variable angle spectroscopic ellipsometer (VASE, wavelength from 1.5 to 4.5 eV, used at angles of 65º and 75º). The results of the thickness measurements on wafers with target oxide thicknesses of 6, 12, 25 and 50 nm can be seen in Table 2-III.

<110> Si wafer ID	Oxidation time [min:s]	Target [nm]	Plasmos [nm]	Woollam M44 [nm]	Woollam VASE [nm]
06nm	01:15	6	6.2 ± 0.5	6.1 ± 0.05	6.3 ± 0.05
12nm	05:30	12	11.9 ± 0.5	11.9 ± 0.04	12.1 ± 0.05
25nm	22:30	25	23.9 ± 0.5	24.1 ± 0.03	24.3 ± 0.05
50nm	75:00	50	49 ± 1	49.0 ± 0.03	49.1 ± 0.05

Table 2-III: *Oxidation times, target and measured dry oxide thicknesses on three different ellipsometer systems.*

The Plasmos ellipsometer is very suitable for locally determining oxide thickness, as it has a programmable (x,y)-stage, as well as a very small spot size (approximately 1 mm in diameter). While the two other systems are supposed to have a greater accuracy (due to the use of multiple wavelengths and angles of incidence), the measured values correspond with those given by the Plasmos ellipsometer.

Figure 2-13 and Figure 2-14 show two measurements of the same wafer: the former was done on the Woollam VASE ellipsometer (measurement spot in the middle of the wafer), the latter is a raster scan, as produced by the Plasmos system.

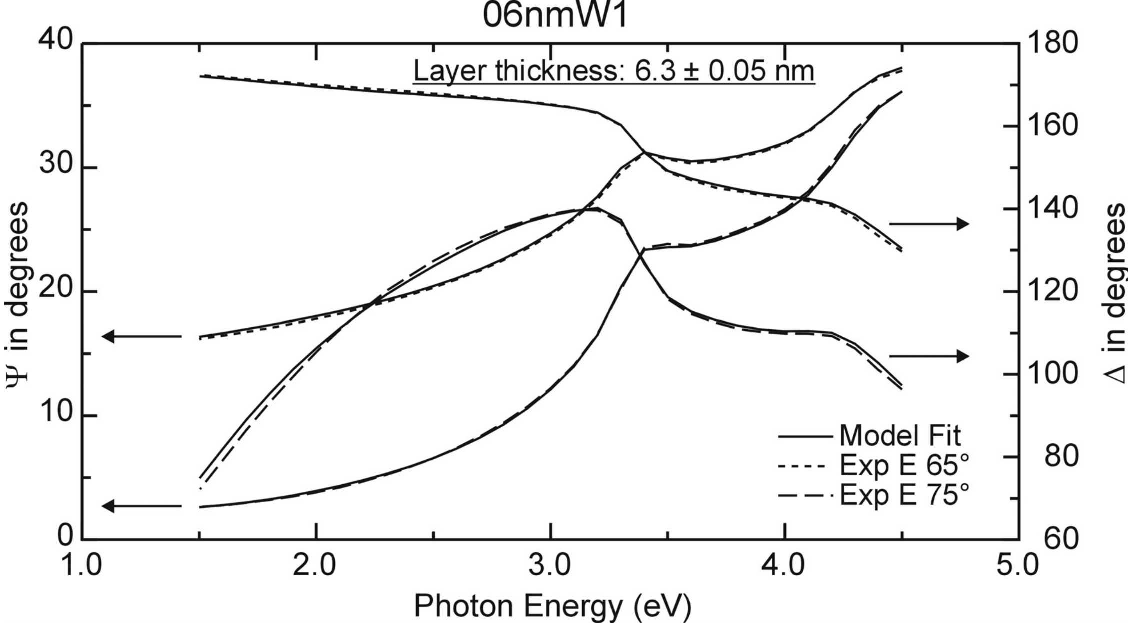


Figure 2-13: *Woollam variable angle spectroscopic ellipsometer data for an oxide layer on <110> silicon, with a measured thickness of 6.3 nm.*

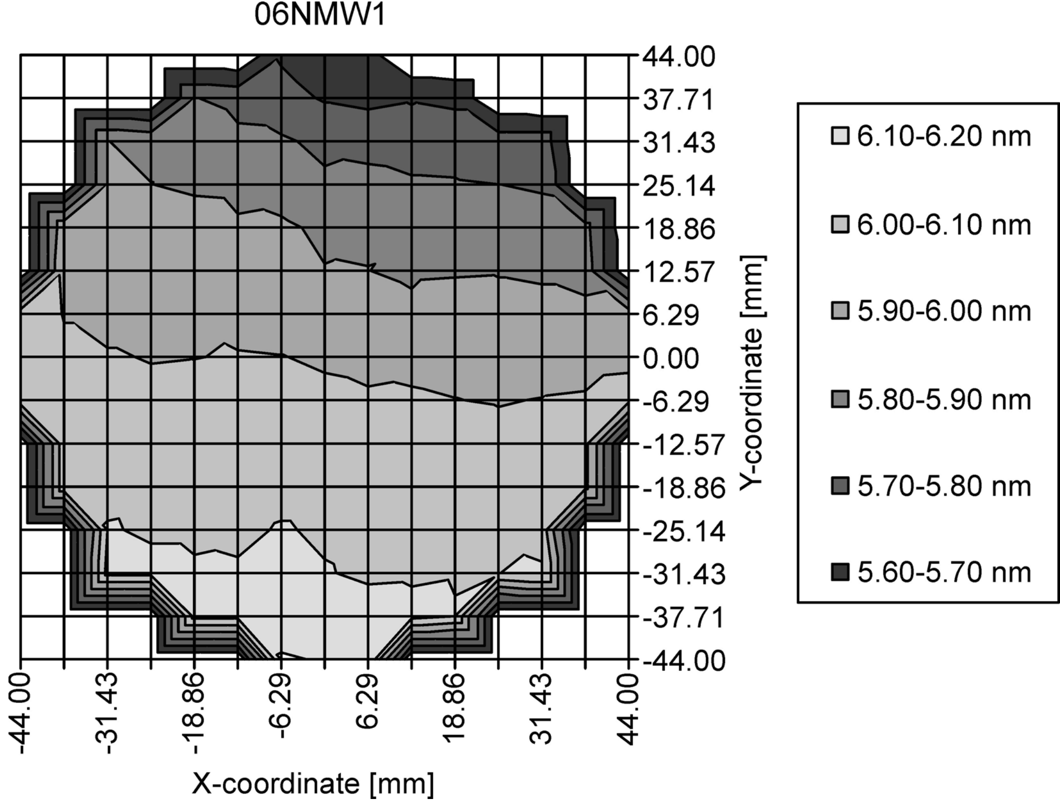


Figure 2-14: *Plasmos raster scan of the same wafer as in Figure 2-13.*

The ellipsometer systems which have been tested all give the same values for oxide thickness, within their experimental errors. However, there is the matter that extremely thin oxide layers have sometimes been observed to have refractive indices that largely deviate from the theoretical value at 632 nm (n = 1.465, which has been assumed in the current experiments). As an example, Hebert et al. [10] found an effective refractive index of 1.9 for ultrathin (4-6 nm) silicon dioxide layers using Fowler-Nordheim tunneling current oscillations and ellipsometry. The idea behind most of the deviations from the bulk value of the refractive index is that a non-instantaneous transition between Si and SiO_2 is assumed. Instead a gradual transition layer with a higher refractive index than oxide, but lower than silicon, is modeled: see Figure 2-15. This results in a lower oxide thickness measurement result. Kao and Doremus, for instance, measured the thicknesses of thin oxide films by Transmission Electron Microscopy (TEM), ellipsometry, and profilometry. The results from these three methods corresponded for thicknesses over 30 nm. When the film thickness was smaller than 30 nm, the thickness as measured by ellipsometry was larger than the values obtained by TEM. The results

could be described by a two-film model, with an interfacial layer of 1.2 nm having a refractive index of 2.5, and a bulk SiO_2 film with the bulk refractive index [11]. Cho et al. [12] presented similar results for SiO_2 layers between 12 and 150 nm. On the other hand, Chao et al. studied sub-10 nm SiO_2 films by variable angle ellipsometry [13], and concluded that an abrupt interface is the most appropriate model, combined with an increase in refractive index, albeit an almost negligible one (they found n = 1.47 for a 10 nm thick film, grown at 950°C).

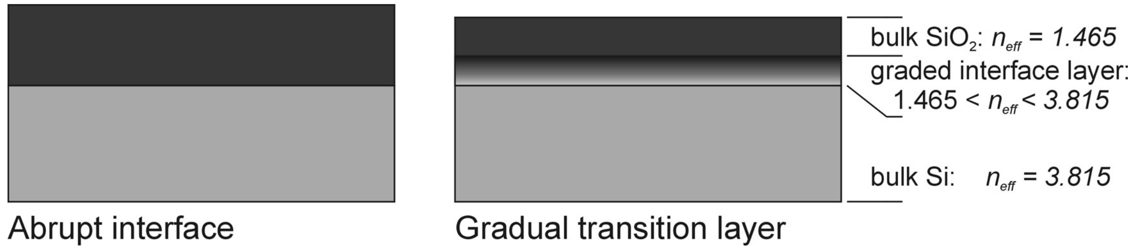


Figure 2-15: *Model for a non-uniform SiO_2 layer: in the picture on the right the physical thickness of the layer is less than would be measured based on the (ideal) model on the left.*

To check whether the physical oxide thickness is really consistent with the ellipsometrically found values, TEM measurements were performed on the four wafers. Pictures of the TEM cross-sections of each of the SiO_2 layers can be seen in Figure 2-16. Each image was calibrated by measuring the distance between the Si <111> planes in the picture: this has to be equal to the literature value of 0.313 nm. After measuring the SiO_2 thickness from the pictures, a comparison between TEM and ellipsometry was made: see Table 2-IV.

Ellipsometer thickness [nm]	**TEM thickness [nm]**
6.1 ± 0.5	6
11.8 ± 0.5	11.1
23.8 ± 0.5	23.6
48 ± 1	47

Table 2-IV: *Comparison between ellipsometer and TEM measurements, indicating reliable ellipsometer values.*

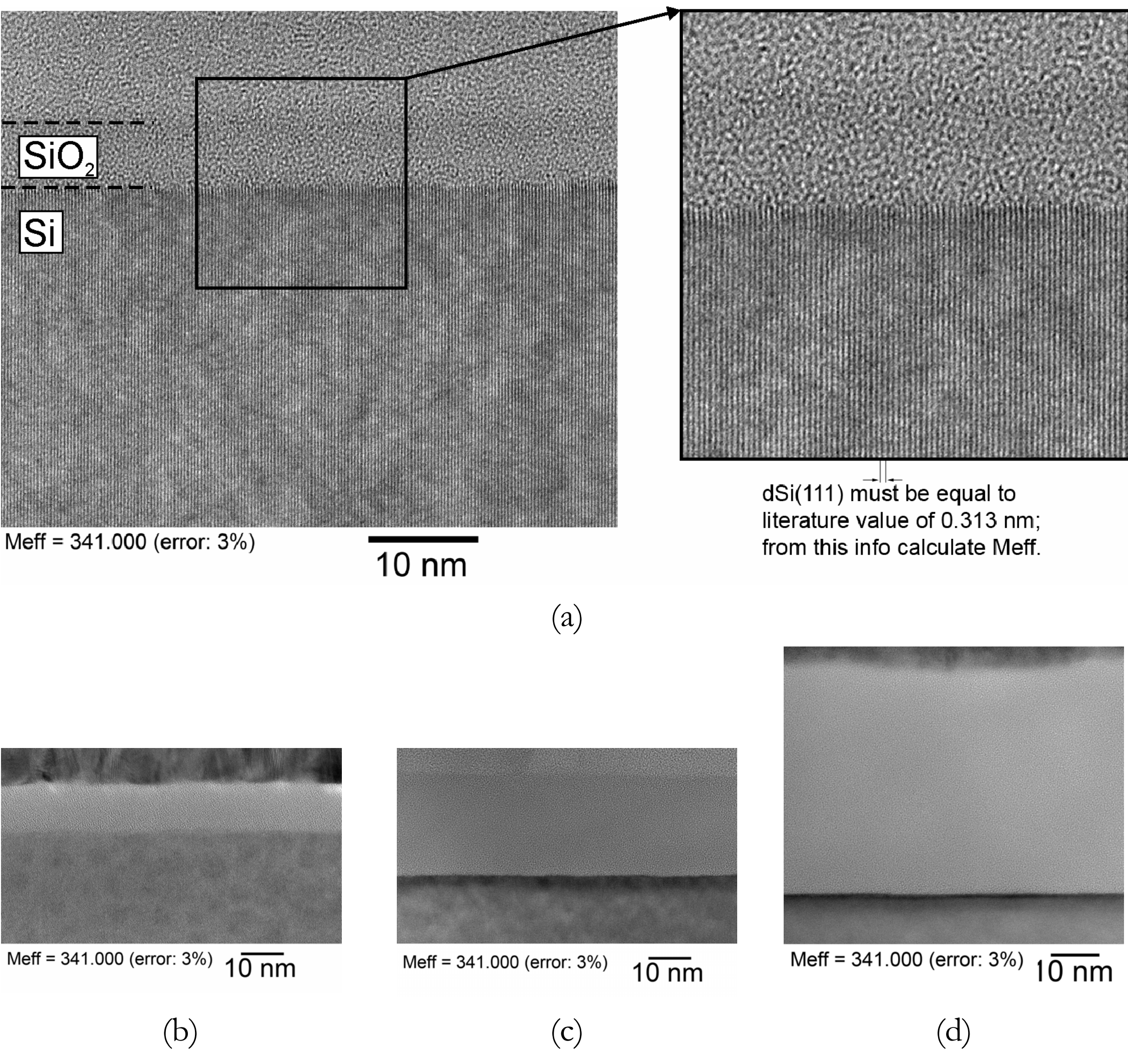


Figure 2-16: *Transmission electron microscope pictures of cross-sections of the dry oxide layers on <110> silicon. (a) 6 nm thickness. (b) 12 nm thickness. (c) 25 nm thickness. (d) 50 nm thickness.*

The conclusion of these measurements is that the ellipsometer measurements correspond with the TEM measurements. The significant deviations in refractive index as found by some other groups, do not seem to occur for these layers.

In summary, well defined dry oxide layers with a thickness of 5-50 nm can be produced by oxidation of Si <110> wafers at a temperature of 950ºC. Characterization of these layers by ellipsometry was shown to be an accurate and reproducible method.

2.2.3 (B)HF etching of channels

Initially, after resist spinning and exposure using a mask containing 4 μm wide lines, followed by a hard bake of the resist, channels were etched in the oxide (wafers with layers of 6, 12, 25 and 50 nm of dry SiO_2) using BHF (NH_4F/HF (1:7)) as the etchant. The etch time was 90 s for all wafers (the etch rate of thermal oxide in BHF is approximately 70 nm/min). All wafers showed a hydrophobic backside after etching, indicating that the oxide layer was completely etched. After etching the photoresist was stripped in fuming nitric acid. Following this, the wafers went through a standard cleaning in nitric acid (10 min in fuming HNO_3, 10 minutes in boiling HNO_3). This standard cleaning forms new layer (1-2 nm) of native oxide on the bottom of the channel. Due to this native oxide growth, the channel depth is decreased with an amount of 0.56 times the native oxide thickness. This is because the native oxide "grows" out of the channel bottom [8]. The expected resulting channel depth can then be predicted by:

$$d_{channel} = d_{dry\ oxide} - 0.56 \cdot d_{native\ oxide} \tag{2.1}$$

After etching in BHF and subsequent wafer cleaning, channel depths were measured using both AFM and ellipsometry (according to equation (2.1)). An AFM picture of one of the resulting steps can be found in Figure 2-17.

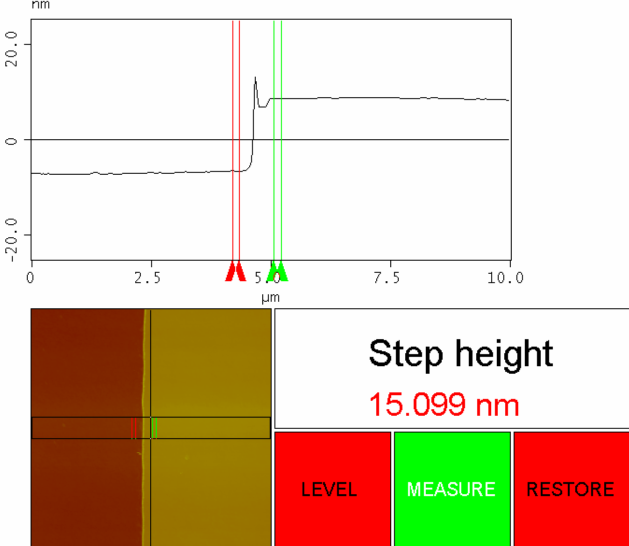


Figure 2-17: *AFM measurement of a step etched in a wafer with an oxide layer with a thickness of approximately 12 nm. The resulting channel depth is larger than expected based on equation (2.1).*

A summary of all measured values can be found in Table 2-V: note that the oxide thickness values differ from those in Table 2-III, because the measurements steps in Table 2-V were not done at the centre position of the wafer, but at another location (the oxide thickness was also measured for this position).

Wafer ID	**Ellipsometer**			**AFM**	**Comparison**
	$d_{dry\ oxide}$ **[nm]**	$d_{native\ oxide}$ **[nm]**	$d_{channel}$ **[nm]**	**Step height [nm]**	**Difference [nm]**
06nm	6.1 ± 0.5	2.2 ± 0.5	4.8 ± 0.8	9.0 ± 0.9	4.2
12nm	11.9 ± 0.5	2.2 ± 0.5	10.7 ± 0.8	15.1 ± 1.5	4.4
25nm	23.9 ± 0.5	2.2 ± 0.5	22.7 ± 0.8	27.2 ± 2.7	4.5
50nm	48 ± 1	2.2 ± 0.5	47 ± 1.3	52.2 ± 5.2	5.6

Table 2-V: *Calculated step heights (based on ellipsometry measurements) compared to measured step heights (measured by AFM) after etching for 90 seconds in BHF.*

From the last two columns, it is obvious that there is a large discrepancy between the ellipsometer-based values and the AFM values. The measurement error in the expected channel depth based on the ellipsometer measurements is approximately 1 nm. The AFM was calibrated using a sample containing 0.39 nm high steps of STO (Strontium Titanate: $SrTiO_3$), the error is estimated to be ± 10% of the measured value.

The explanation for the differences in expected and measured values could be that the BHF does not stop exactly on the interface of silicon and silicon dioxide, but that it etches further, into the "bulk" silicon. Therefore the etching behavior of BHF in comparison to various concentrations of HF was investigated.

2.2.4 BHF overetch determination

For an investigation into the etching behavior of (B)HF on thin oxide layers, an experiment was designed to compare the influence of etching with various solutions (BHF, 1% HF, 2% HF, 5% HF). The general idea behind the experiment can be seen in Figure 2-18.

The process consists of the following steps:

1. Dry oxidizing <110> Si wafers.
2. Photolithography (4 μm lines and spaces mask).
3. (B)HF etching of the dry oxide layer.
4. Standard cleaning of wafers.
5. AFM measurement of step height ($d_{AFM\ step}$).
6. Strip the sample in the same time (and in the same etching solution) as in step 3.
7. AFM step height measurement after stripping ($d_{AFM\ after\ strip}$).

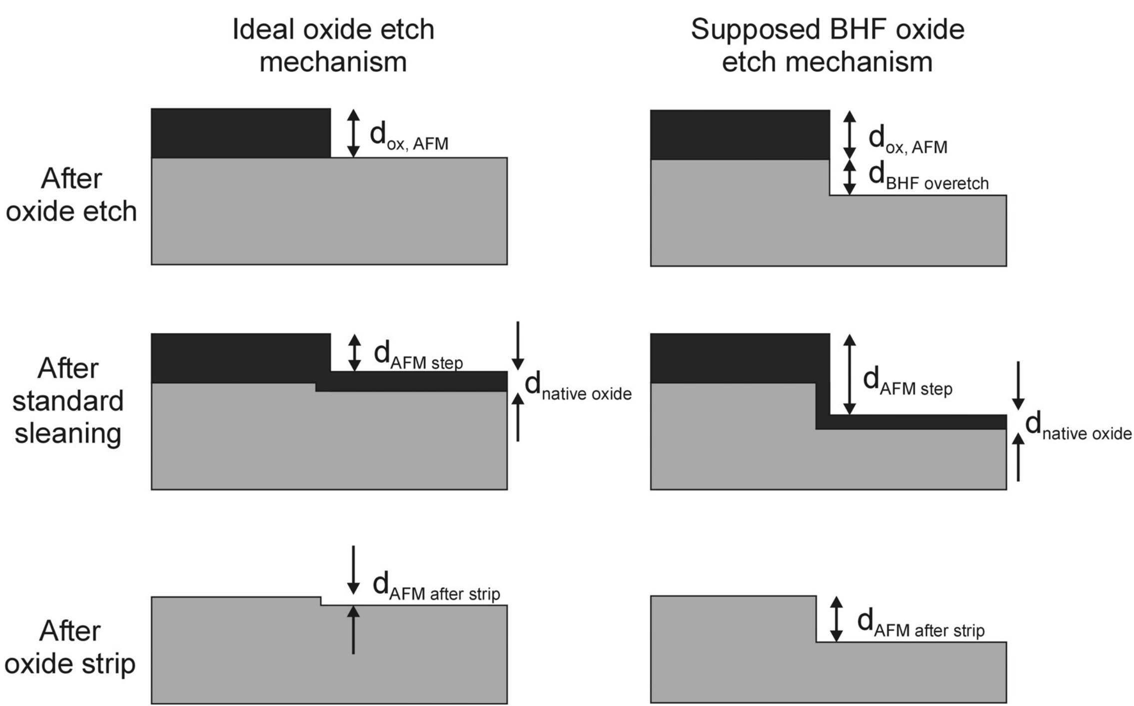


Figure 2-18: *Left: ideal etching mechanism, stopping exactly on the silicon/oxide interface. Right: proposed BHF oxide etching effect: after hitting the interface, the etching continues into the silicon substrate, creating a deeper trench.*

Note that even in the case of exactly stopping the etching on the interface, the sample should show a step under the AFM after stripping, due to the formation of native oxide (typically 1-2 nm) on the exposed silicon surface (the "bottom" of the channel)). The formation of this native oxide consumes a fraction of the silicon wafer (to be precise: the amount of consumed silicon is 0.44 times the native oxide thickness). Any steps significantly larger than 1 nm after the oxide strip, can not

originate from the formation and stripping of the native oxide alone and must therefore have a different cause.

The following equations are proposed to describe the experiments (see Figure 2-18 for an explanation of the different step heights):

1% HF solution:

$$d_{AFM\ after\ strip} = 0.44 \cdot d_{native\ oxide} \tag{2.2}$$

$$d_{ox,\ AFM} = d_{AFM\ step} + 0.56 \cdot d_{native\ oxide} \tag{2.3}$$

BHF solution:

$$d_{AFM\ after\ strip} = d_{BHF\ overetch} + 0.44 \cdot d_{native\ oxide} \tag{2.4}$$

$$d_{ox,\ AFM} + d_{BHF\ overetch} = d_{AFM\ step} + 0.56 \cdot d_{native\ oxide} \tag{2.5}$$

For etching in 1% HF, the value for the step height measured by AFM after stripping the wafer in BHF ($d_{AFM\ after\ strip}$) was used to calculate the native oxide thickness ($d_{native\ oxide}$), i.e. the native oxide that was grown during the stripping of the photoresist and the subsequent standard cleaning step after the trench etching step. The step height after stripping (0.7 nm) gives us a native oxide thickness of 1.6 nm, which is a realistic value. To estimate the thickness of the oxide layer, based solely on AFM measurements ($d_{ox,\ AFM}$), equation (2.3) can be used.

For the BHF etched samples, $d_{BHF\ overetch}$ is first calculated with equation (2.4), using the calculated value of 1.6 nm for the native oxide thickness and the measured step height after stripping ($d_{AFM\ after\ strip}$): the value for $d_{BHF\ overetch}$ is then entered into (2.5) to calculate the oxide thickness, based on the AFM measurements ($d_{ox,\ AFM}$).

The results of the performed measurements, using a wafer with a SiO_2 layer of approximately 12 nm, can be found in Table 2-VI. The etch times are defined as the time it took for the sample to become hydrophobic, plus a 10 seconds overetch, (to ensure that the layer was etched completely). An exception is the “BHF + 75s”, which was etched for 90 seconds (the same time as the wafers in Table 2-V, where the presumed effect was first observed).

etchant	etch [s]	$d_{AFM\ step}$ [nm] *(measured)*	$d_{AFM\ after\ strip}$ [nm] *(measured)*	$d_{BHF\ overetch}$ [nm] *(calculated)*	$d_{ox,\ AFM}$ [nm] *(calculated)*	$d_{ox,\ ellipsometer}$ [nm] *(measured)*
1% HF + 10 s	205	11.8 ± 1.2	0.7 ± 0.1	0 (assume)	12.7 ± 1.5	11.5 ± 0.5
2% HF + 10 s	95	11.7 ± 1.2	0.7 ± 0.1	0 (assume)	12.6 ± 1.5	11.5 ± 0.5
5% HF + 10 s	32	11.9 ± 1.2	0.7 ± 0.1	0 (assume)	12.8 ± 1.5	11.5 ± 0.5
BHF + 10 s	25	12.5 ± 1.3	1.6 ± 0.2	0.9 ± 0.4	12.5 ± 1.7	11.5 ± 0.5
BHF + 75 s	90	14.3 ± 1.4	3.3 ± 0.3	2.5 ±0.5	12.7 ± 1.9	11.5 ± 0.5

Table 2-VI: *BHF overetch influence experiment. The "$d_{ox,\ ellipsometer}$" value is the thickness of the initial dry oxide layer, measured by the Plasmos ellipsometer.*

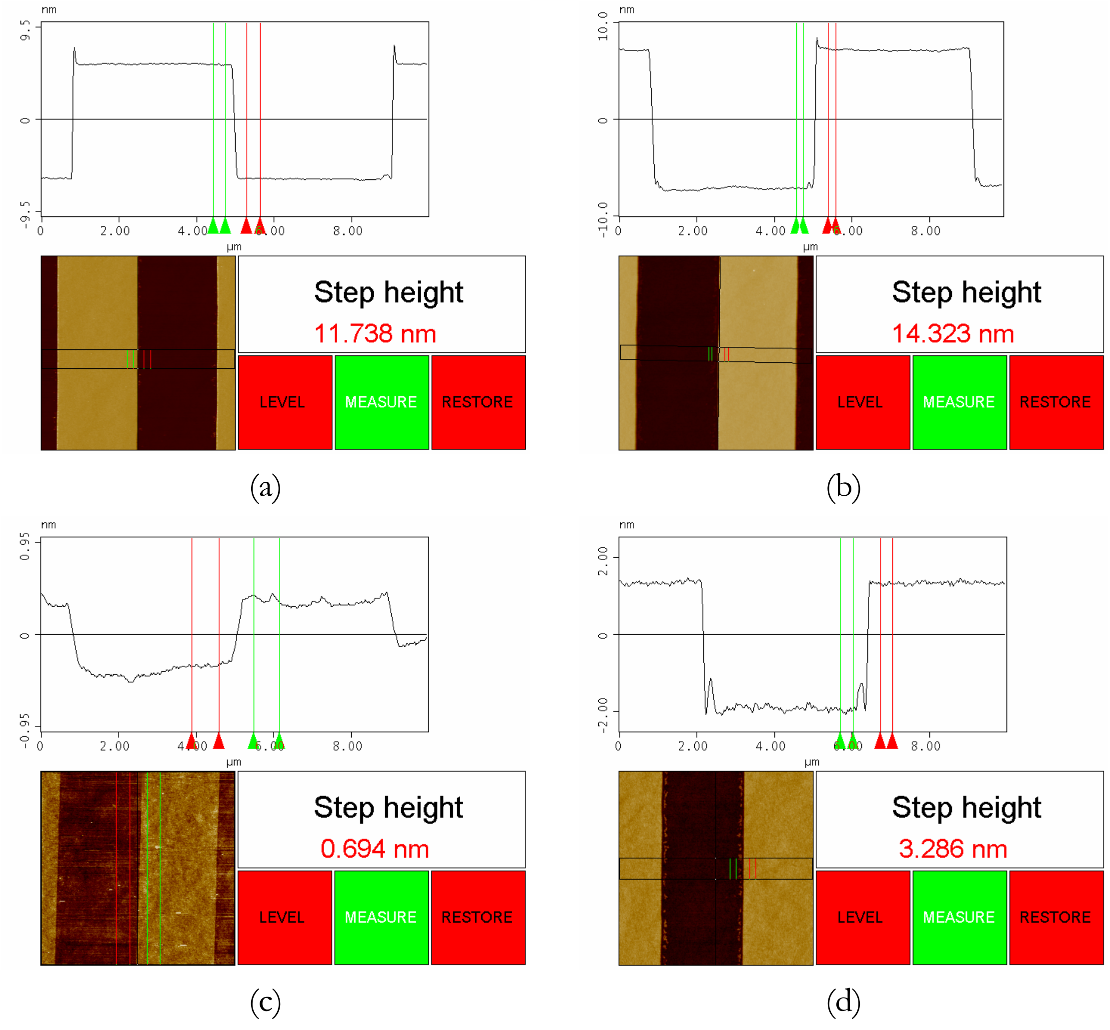


Figure 2-19: *AFM step measurement before and after stripping. (a)/(c) 205 s 1% HF etching before/after stripping. (b)/(d) 90 s BHF etching before/after stripping. Notice the large step due to the BHF overetch in (b).*

In Figure 2-19 the step height after etching, cleaning and stripping with 1% HF and BHF (90 seconds) can be seen: clearly the BHF etch step of 90 seconds has a different effect than the 1% HF etch process. From the obtained results the following conclusions can be drawn:

1. The diluted HF solutions seem to stop exactly on the Si/SiO_2 interface: there is no significant difference between 1, 2 and 5% HF. This was also observed for a wafer with 48 nm of SiO_2 (note that 2% and 5% HF are aggressive etchants: delaminating of photoresist occurs when etching 48 nm SiO_2 layers).
2. For the 1, 2 and 5% HF samples, the measured value for $d_{AFM\ after\ strip}$ is the amount of silicon which was consumed to grow the native oxide layer during standard cleaning: this indicates a native oxide thickness of 1.6 nm
3. Overetching with BHF solution gives rise to an extra etch into the silicon substrate; this is time dependent (compare “BHF + 10s” and “BHF + 75s”).
4. For the BHF etched samples, the measured value for $d_{AFM\ after\ strip}$ is composed of a part which is due to the native oxide formation/removing (see point 2), and a part which is due to overetching into the substrate.
5. The ellipsometer measurements for the oxide thickness and the calculated $d_{ox,\ AFM}$ values correspond within the experimental errors.

2.2.5 Bulk etching of silicon using 1% HF and BHF

To confirm that the BHF actually etched silicon (albeit at a very slow rate), and that this effect is of importance in the fabrication of fluidic nanochannels, an experiment was done to directly compare the bulk etch rates of Si <110> and <100> both in 1% HF and in BHF (for various etch times). To do this, four <110> and four <100> double side polished silicon wafers were weighed on a Mettler scale (with an accuracy of ± 10 μg), together with one calibration wafer (which was not processed in any way, but was just used to check the consistency of the scale from measurement to measurement). After weighing, the wafers were subjected to the following routine (in this example 1% HF is used as the etchant, with an etch time of 30 s):

1. Etch one <110> and one <100> wafer in 1% HF for 30 seconds.
2. Rinse wafers in DI water.
3. Oxidize wafers: 1 min in 70% HNO_3 @ 95°C.
4. Rinse wafers in DI water, spin-dry, go to step 1.

A total of five cycles were done for each wafer pair and for each etchant/time. The results of the weight differences before/after etching can be found in Table 2-VII.

wafer	5*30 s 1% HF	5*2 s BHF	5*90 s BHF	5*300 s BHF
<110> Si	120 ± 20 μg	110 ± 20 μg	440 ± 20 μg	930 ± 20 μg
<100> Si	130 ± 20 μg	150 ± 20 μg	330 ± 20 μg	650 ± 20 μg

Table 2-VII: *Weight difference before and after etching silicon wafers in 1% HF or BHF for various times.*

The mass of a four inch, 525 μm thick silicon wafer is 9.5 g. This is equivalent to 0.55 nm per 10 μg. With the use of this mass-thickness conversion, and keeping in mind that the wafers are etched 5 times and at two sides per wafer, this gives the following silicon removal rate per side, and per cycle:

wafer	30 s 1% HF	2 s BHF	90 s BHF	300 s BHF
<110> Si	0.66 ± 0.11 nm	0.61 ± 0.11 nm	2.42 ± 0.11 nm	5.12 ± 0.11 nm
<100> Si	0.72 ± 0.11 nm	0.83 ± 0.11 nm	1.82 ± 0.11 nm	3.58 ± 0.11 nm

Table 2-VIII: *Silicon removal rate per cycle for etching in 1% HF and BHF for various times.*

The values in Table 2-VIII are not the actual etch rates of the silicon, but the total change due to the etching of the native oxide layer (which is re-grown in step 3 of each cycle) and the actual etching of bulk silicon in the solution. To compensate for the SiO_2-component in Table 2-VIII, the etch rates of silicon <110> and <100> in 1% were measured for an etch time of 60 minutes. This yielded an etch rate of practically zero for both silicon wafers. This leads to the conclusion that all of the silicon which is effectively removed in 1% HF (0.66 nm for <110> Si, and 0.72 nm for <100> Si), was in the form of SiO_2. These values should therefore be subtracted from all values in Table 2-VIII, giving the final bulk silicon etch rates, which are presented in Table 2-IX.

wafer	30 s 1% HF	2 s BHF	90 s BHF	300 s BHF
<110> Si	0.00 ± 0.22 nm	-0.05 ± 0.22 nm	1.76 ± 0.22 nm	4.46 ± 0.22 nm
<100> Si	0.00 ± 0.22 nm	0.11 ± 0.22 nm	1.10 ± 0.22 nm	2.86 ± 0.22 nm

Table 2-IX: *Bulk silicon etch rates per cycle for etching in 1% HF and BHF for various times.*

These values are in general agreement with the ones found in the previous paragraphs. The etch rate ratio of <110>:<100> is approximately 1.6:1. A possible explanation for this are the differences in surface atom concentration and oxidation ratio between both orientations:

Si surface atom concentration:	{110}:{111}:{100} ~ 1.41:1.15:1.0
Available bond density:	{110}:{111}:{100} ~ 1.41:1.15:2.0
Oxidation ratio:	{110}:{111}:{100} ~ 1.50:1.40:1.0

Based on these figures, the most probable explanation for the etching of silicon in buffered HF solutions is that there is a constant oxidation/oxide removal reaction taking place at the silicon surface.

2.2.6 TEM measurements of the BHF overetch effect

Finally, to confirm the BHF overetch effect, TEM cross-sections of the BHF etched channels were made: a picture of such a channel can be seen in Figure 2-20. In this figure the “BHF overetch” effect is actually visible: the trench slopes lightly downward when traveling from right to left along the picture.

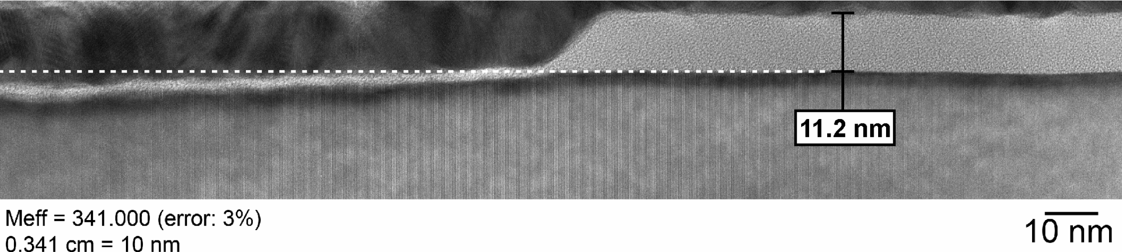


Figure 2-20: *TEM measurements of a step etched (90 seconds BHF etch) in an oxide layer which was originally 11.8 nm in thickness (ellipsometer measurement).*

2.2.7 Direct bonding procedure to silicon and Borofloat glass

Again, the bonding of the patterned wafers to other silicon or Borofloat wafers proved to be straightforward. After standard fuming and boiling HNO_3 cleaning, followed by a Piranha cleaning step, the wafers bonded spontaneously and completely when brought in contact with each other. This shows once more that

the dry oxide layer has excellent smoothness, as this is a requirement for direct bonding [14]. After annealing only very few bonding defects could be observed.

2.2.8 Channel fabrication and bonding results

Fabricated channels and surface roughness

After processing, the resulting channels were imaged by AFM. AFM measurements of a channel etched with 1% HF, using a 6 nm dry oxide spacer layer, can be found in Figure 2-21. The measured stepheight was 5.7 ± 0.6 nm.

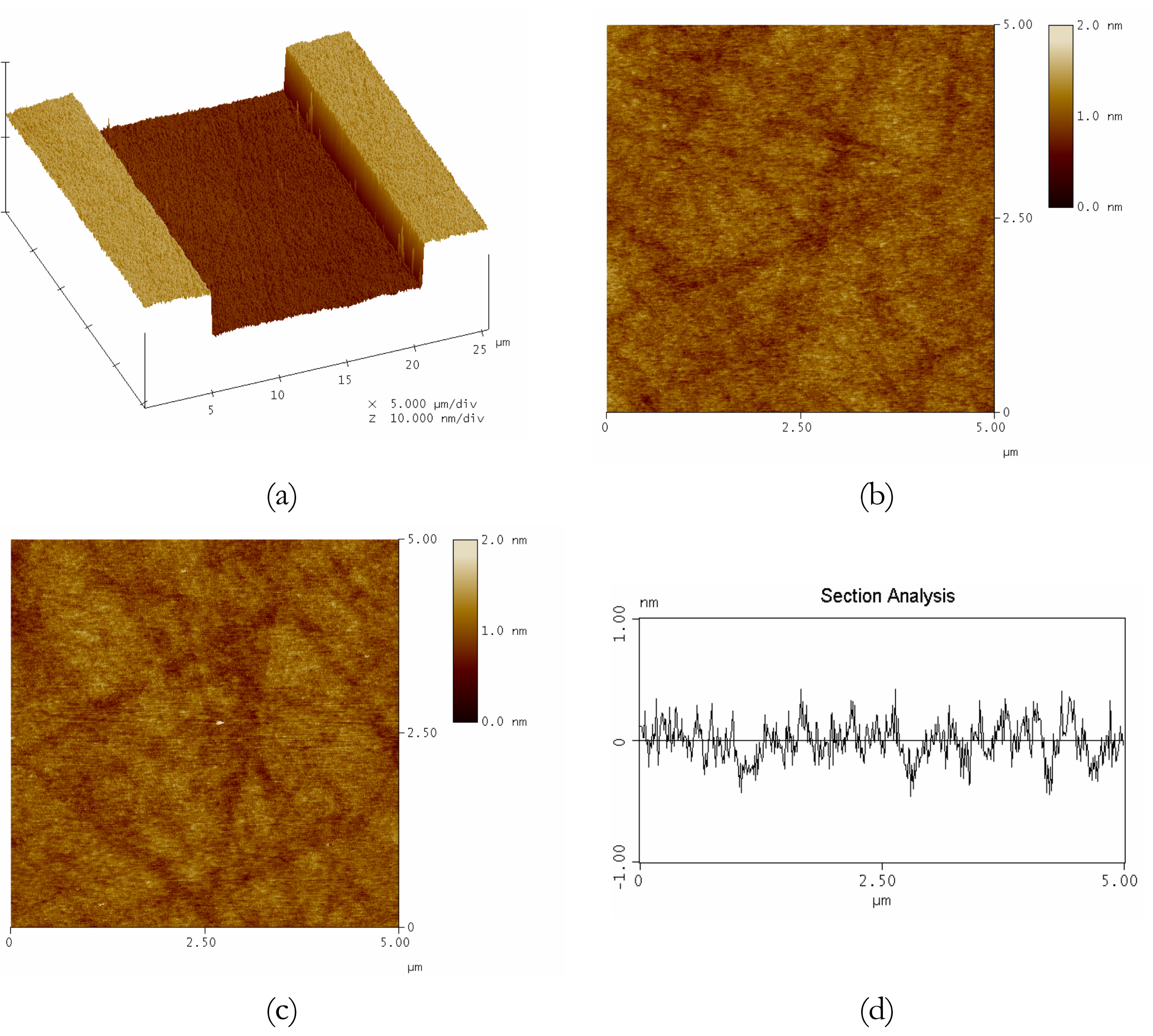
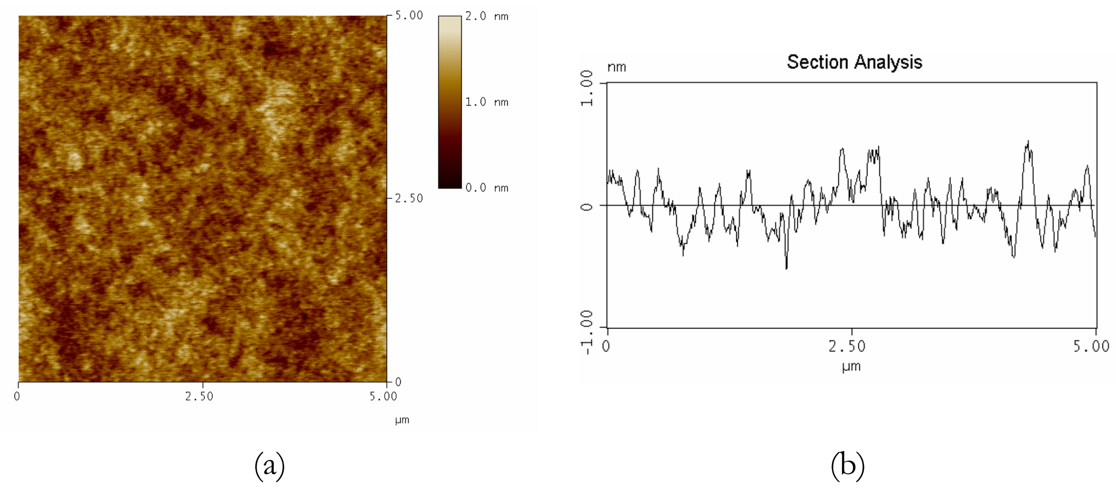


Figure 2-21: *AFM scans of a channel etched with 1% HF in an oxide layer with an initial thickness of 6 nm. (a) 20 micrometer wide nanochannel. (b) Roughness scan of the top of the channel. (c) Roughness scan of the bottom of the channel. (d) Section view of (c).*

The surface roughness on the bottom of the channel was measured on an area of 5 by 5 µm and was found to have a value of 0.16 nm RMS (or 0.13 nm R_a). There was no measurable difference in roughness between the initial dry oxide layer and the bottom of the etched trench, as can be seen in Figure 2-21(b/c).

The roughness of the bonding side of the Borofloat wafers was also measured. It has a value of 0.22 nm RMS, or 0.18 nm R_a. The AFM scan of the Borofloat wafer surface, together with a section view of the scan can be found in Figure 2-22.

The measured roughness values are all very low, as was expected (and necessary for the direct bonding procedure).



(a) (b)

Figure 2-22: *AFM scans of the bonding side of a Borofloat wafer. (a) Surface roughness scan. (b) Section view.*

Cross-sections of bonded wafers

In Figure 2-23 two pictures of the cross-section of an array of nanochannels can be seen. These were fabricated by growing a 10 nm layer of dry oxide on Si <110> wafers, pattering this layer in a 1% HF solution using a pattern in photoresist as the mask material (consisting of 4 µm lines and spaces), and bonding to a second <110> silicon wafer. After the anneal step (1100°C for bonding to silicon and 400°C for bonding to Borofloat) the wafer was cleaved and cross-section SEM pictures were taken.

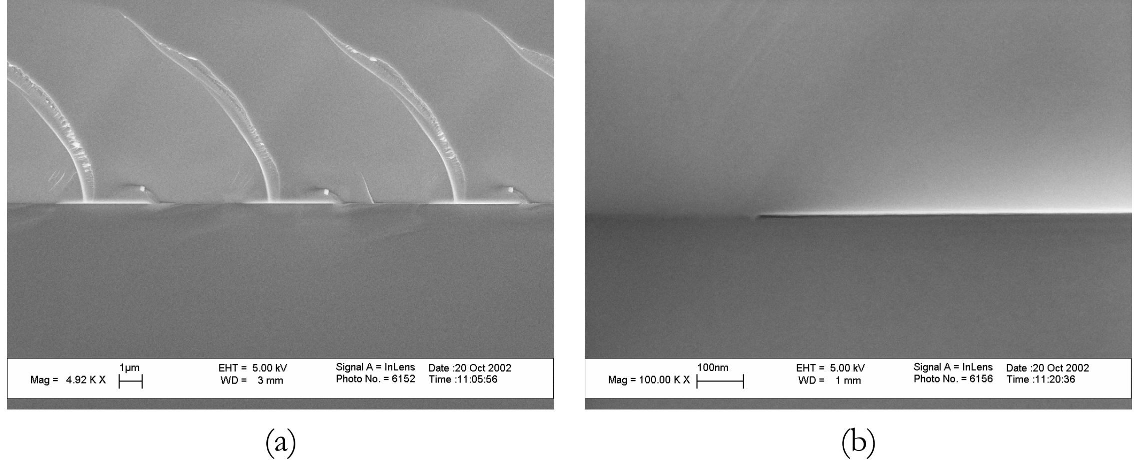


Figure 2-23: *SEM cross-sections of nanochannels fabricated by patterning a 10 nm layer of SiO_2 in 1% HF and subsequent bonding of the wafer to a silicon cover wafer.*

All channels were observed to be open over the entire width of the channel. An accurate direct channel height measurement can not be done based on these SEM pictures, but the estimated channel height is certainly in the order of 10 nm.

2.3 Conclusions

Anisotropic wet etching of <110> silicon can be used to created fluidic nanochannels with a depth up to 500 nm, using the native silicon dioxide layer of the wafer as a mask material. For deeper trenches, a dedicated mask layer should be deposited beforehand, e.g. by oxidation or silicon nitride deposition.

OPD 4262 positive resist developer, containing 2.5% TMAH, is an excellent etchant which couples a very smooth surface finish of the etched structures (the surface roughness on the bottom of the channels is approximately 0.3 nm RMS), to a well controllable etch rate of approximately 3.7 nm/min at room temperature (for Si <110>). The resulting channels have a rectangular cross-section, and show good uniformity (approximately ± 1 nm variation in channel depth for a wafer with 4 µm wide and 50 nm deep trenches across the complete wafer surface).

Dry oxidation of Si <110> wafers, in combination with 1% HF or BHF etching, is a suitable technology to create nanochannels with a depth below 50 nm. When using BHF as an etchant, care must be taken not to overetch the samples too long, as this will create a deeper trench than expected. 1% HF etched channels do not

suffer from this overetch effect. However, 1% HF is more aggressive to photoresist, which could lead to failure. More concerning these issues will be addressed in the next chapter, which deals with the fabrication of chips for fluidic measurement, using the developed technology from the present chapter. The resulting channels after 1% HF etching have a very low surface roughness (RMS value below 0.2 nm).

Summarizing, we have two complementary technologies for creating nanochannels. The OPD 4262 based process has the advantage of vertical sidewalls after etching, which is of importance when the width of the channels is reduced (even then a rectangular channel cross-section is preserved). Also, creating a channel in bulk silicon can have advantages for further processing of the wafer, depending on the desired application. Finally, an appealing feature of the OPD 4262 etched channels is the very low underetch rate, making reduction of the channel width possible.
The dry oxide nanochannels fabrication method has the advantage of being able to accurately create and characterize very shallow (sub-10 nm) channels with extremely smooth surface finish, which is difficult when using the wet anisotropic etching process. On the downside, no rectangular cross-sectioned channels can be produced, due to the isotropic oxide etching character of the (B)HF. However, when the channel width is above 1 micrometer, the large width-height aspect ratio makes this isotropic etch profile at the edges of the channel of negligible importance.

2.4 References

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3

Nanochannel chip fabrication

After discussing the etching techniques in the previous chapter, in this chapter a fluidic chip will be designed and fabricated, containing 1D nanochannels. Chips will be made either by the bulk wet anisotropic etching of <110> silicon (in OPD 4262), or by patterning an ultrathin dry oxide layer (as thin as 6 nm). Also, fluid reservoirs, measurement rulers and external fluidic connections will be incorporated in the design.

3.1 Chip design

A chip containing nanochannels, fluidic inlet/outlet reservoirs, powder blasted access holes and measurement rulers has been designed. For the layout of such a chip, see Figure 3-1.

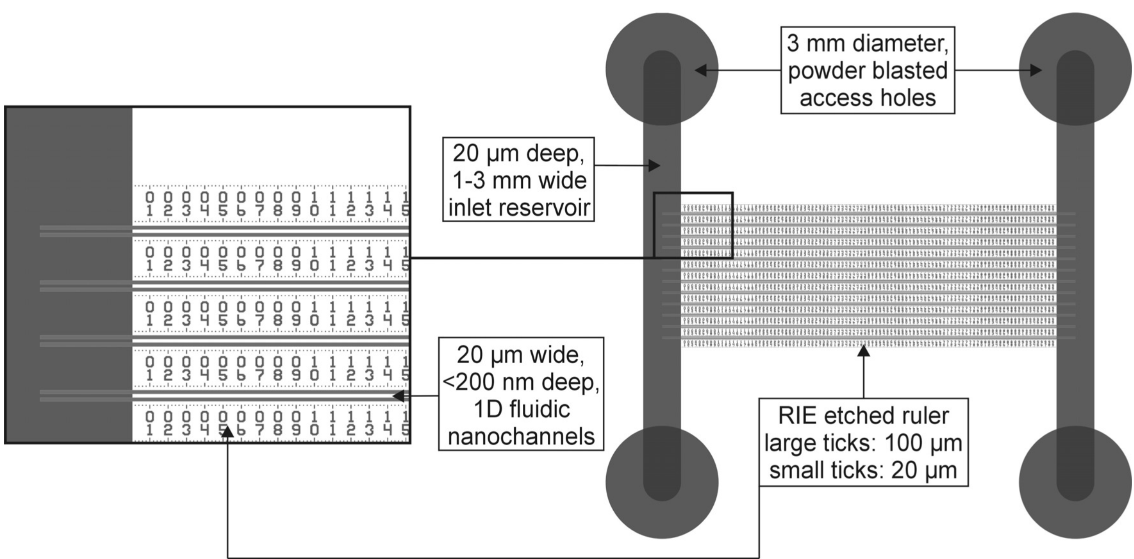


Figure 3-1: *Chip design for 1D fluidic nanochannels (the total length of each nanochannel is 1 cm).*

In addition to the nanochannels, the chips contain large (1-3 mm wide, 20 μm deep) inlet and outlet reservoirs, and powder blasted access holes (3 mm in diameter) to manually insert fluids into the chip. There are two holes for the inlet reservoir: one for the filling of the chip, the other one functions as an air exhaust. At the outlet there are also two holes, so the chip could be filled from both sides. Alongside the fluidic nanochannels, rulers and tick marks are etched, to be able to very accurately measure the position of the fluid in the channel during capillary filling experiments.

In the following paragraphs chip fabrication and characterization, using the two different fabrication methods, will be discussed.
The process documentation used for the fabrication of the chips can be found in the Appendix.

3.2 Fabrication of chips using wet anisotropic etching of <110> silicon

Chips containing nanochannels with a depth of 50, 100 and 150 nm were fabricated according to the wet anisotropic etching process described in paragraph 2.1.

3.2.1 Fabrication procedure

The complete chip fabrication sequence is depicted in Figure 3-2.

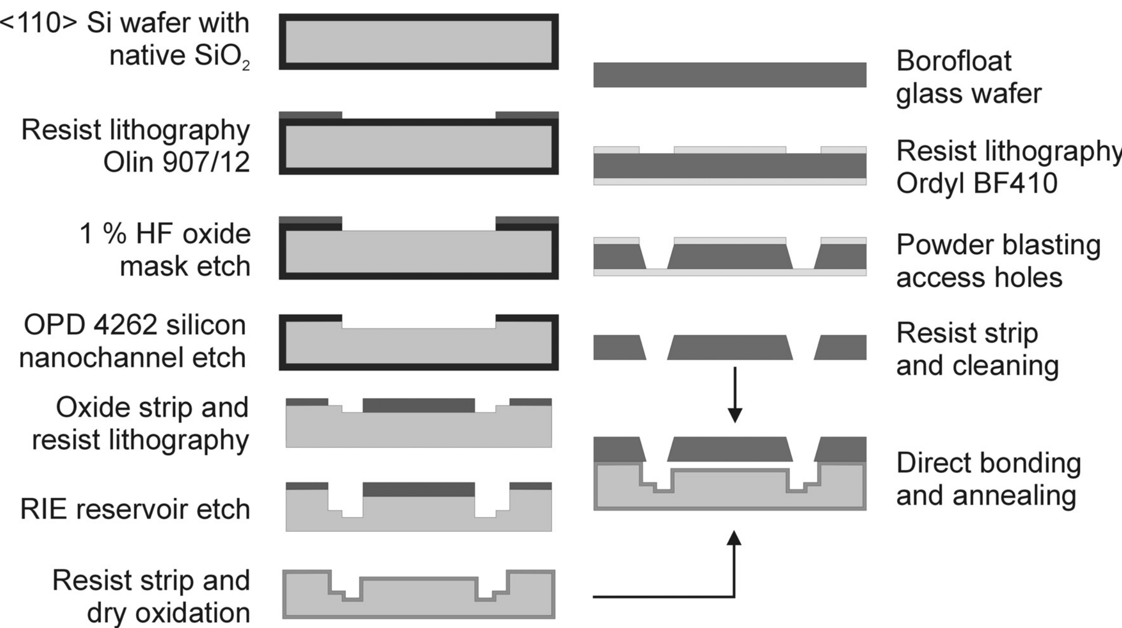


Figure 3-2: *Fabrication process for creating nanochannel chips, using wet anisotropic etching of <110> silicon.*

A <110> p-type silicon wafer was used as the bottom wafer. A standard cleaning step (10 minutes in fuming nitric acid, followed by 10 minutes in boiling nitric acid) was performed before the first lithographic step. After a dehydration step (>10 min at 120ºC), an adhesion layer (HMDS) and photosensitive resist (Olin 907/12) were spin-coated (20 seconds at 4000 rpm). Then, after a softbake (1 min at 95ºC), the resist was exposed (3.5 sec at 12 mW/cm^2) using an ElectroVisions 620 exposure apparatus (EVG), and a mask containing the 1D nanochannel structures (20 µm wide, 1 cm long lines). After this, a post exposure bake (1 min at 120ºC) was performed, followed by development of the exposed resist by a standard 2.5% water diluted TMAH solution (Olin OPD 4262 positive resist developer).

After lithography, a 1% HF dip (1 min) was done to transfer the resist pattern to the native oxide layer. Then the wafer was immersed in acetone for one minute to strip the resist, directly followed by an isopropanol (IPA) cleaning dip (1 min), after which the wafer was quickly spin-dried (approximately 10 seconds).

The pattern transfer into the native oxide was directly followed by a wet anisotropic silicon etch step at room temperature using a fresh OPD 4262 solution as the wet chemical etchant and the native oxide as the mask material [1]. Finally, the wafer was rinsed with DI water and spin-dried.

After this, the micro reservoirs (length: 1 cm, width: 1 or 3 mm) and the measurement rulers were defined using Olin 907/12 as the resist, with an additional hard bake (30 min at 120ºC, followed by 15 minutes at 150ºC) after the development step. The reservoirs were etched on an Oxford Plasmalab 100 RIE apparatus (T = -110ºC, 120 sccm SF_6, ICP power 600W, V_{DC} = -16V, etch rate ≈ 4 μm/min) for 5 minutes. This provided an approximate depth of 20 μm.

After a surface scan with a mechanical profiler (Sloan Dektak II) to determine the approximate depth of the silicon nanochannels, the wafer was oxidized at 950ºC for 15 minutes to grow a dry oxide layer of about 20 nm (to ensure that the resulting channel is totally hydrophilic: this is of importance in the filling experiments to come). After oxidation the silicon bottom wafer was ready for the bonding steps.

For the top wafer a Borofloat glass wafer was used (suitable for direct bonding, because of its very low surface roughness). It was covered with Ordyl BF410 negative powder blasting resist foil on both sides (the direct bonding side was covered first, to protect it from scratching during the powder blasting procedure, which is carried out outside the clean room, and involves a lot of dust). Then the other side was laminated and exposed using a Karl Süss mask aligner for 20 seconds at 9 mW/cm^2 and a mask with the access holes. The resist was then spray-developed in a 0.2% Na_2CO_3-solution for 3 minutes and holes were powder blasted [2] in the glass. The powder blasting foil was removed by hand and the wafers were ultrasonically cleaned in acetone for 15 minutes to remove any remaining resist and

loose particles. After DI rinsing and drying the wafer was ready for the bonding procedure.

Before bonding, both the top wafer and the bottom wafer underwent a standard cleaning step, as well as an additional Piranha step (>10 minutes in H_2SO_4:H_2O_2 (3:1) solution, at a temperature of 130ºC) to clean the silicon and the Borofloat glass surface. Finally, the wafers were spin-dried, manually aligned (the alignment was non-critical, due to the large size of the powder blasted access holes) and bonded. After prebonding, the bond was annealed at 400°C for 4 hours. This annealing temperature of the silicon-to-glass bond is sufficiently low to prevent plastic deformation of the glass (and thereby possibly closing of the nanochannels).

3.2.2 Fabrication results

A picture showing the 1D nanochannels, together with the RIE etched reservoirs and the measurement rulers, can be seen in Figure 3-3.

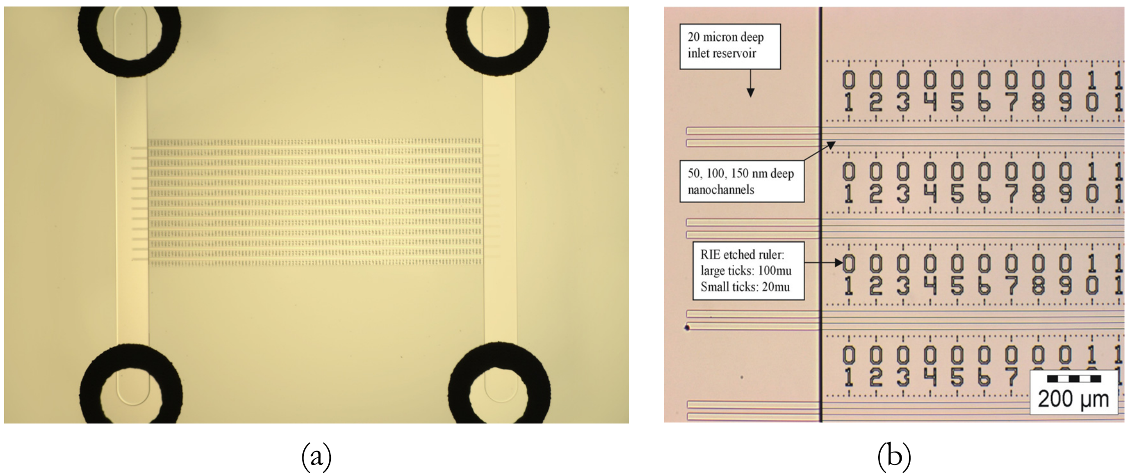


Figure 3-3: *Optical microscope pictures of fabricated capillary filling chips. (a) Complete chip view. (b) Close-up: the 20 µm wide nanochannels, 1 mm wide reservoirs and the ruler structures are clearly visible.*

A calibration of the etch rate of the nanochannels in <110> silicon using OPD 4262 at room temperature with this mask showed that the etch rate was approximately 2.8 nm/min. This is a lower etch rate than previously determined in the etch rate calibration (3.7 nm/min). This could be caused by the fact that the chip design differs from the mask used in the previous experiments (which had 4 micrometer lines and spaces, over the full wafer). Also, temperature conditions in

the clean room are not always constant. (the temperature of a freshly poured beaker of OPD 4262, exposed to the forced convection inside a laminar flow cabinet, was observed to decrease from 20.5ºC to 18.9ºC over a period of six hours, and dropped to 18.5ºC after 27 hours. As a result, the etching times to obtain 50, 100 and 150 nm deep channels were 18 min, 36 min and 55 min, respectively.

The reactive ion etching yielded 20 μm deep inlet reservoirs and rulers (measured with a Dektak surface profiler). The dry oxidation step produced a layer of silicon dioxide of 19nm, as was determined by ellipsometric measurements on a Plasmos SD 2002 ellipsometer (at a refractive index of 1.465 for SiO_2).

After the dry oxidation, the depth of the channels on each wafer was measured using a Dektak surface profiler. For each of the ten chips on a wafer, the depth of the top, the middle, and the bottom channel was measured (for measurement locations: see Figure 3-4). The results of these measurements are given in Figure 3-5 and Table 3-I.

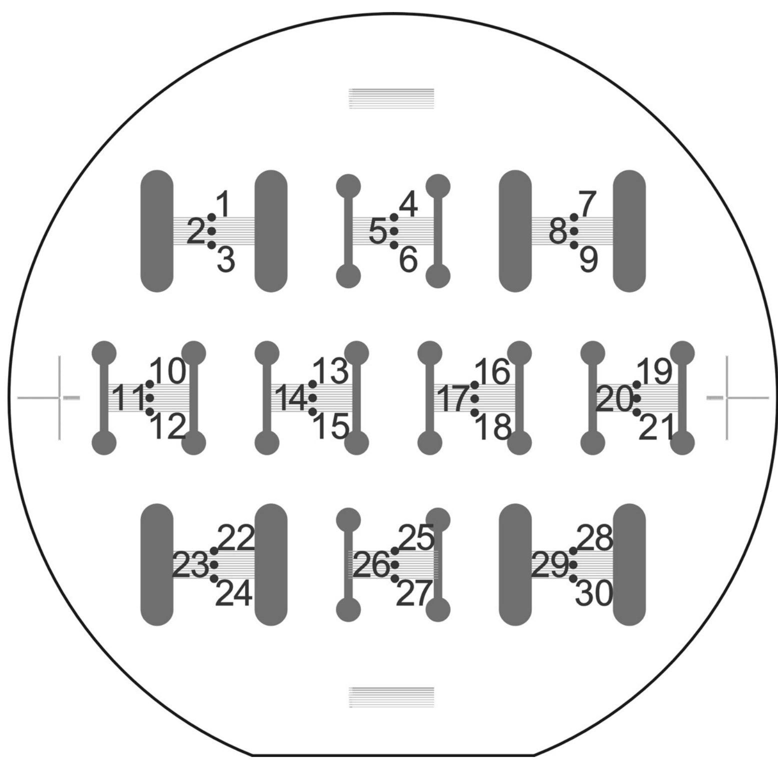


Figure 3-4: *Channel depth measurement locations.*

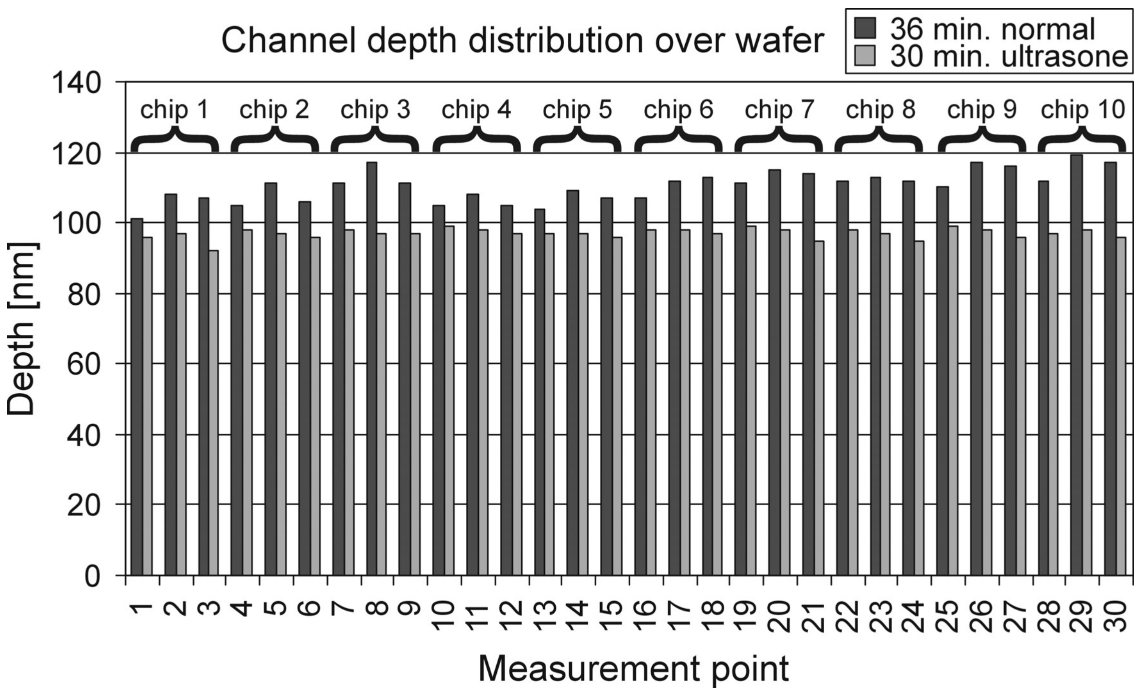


Figure 3-5: *Channel depth distribution over the wafer, according to measurement points defined in Figure 3-4.*

Etch time [min]	Average depth [nm]	Std. dev. [nm]	Minimum [nm]	Maximum [nm]	Etch rate [nm/min]
18	54	2.1	51	59	3.0
36	111	4.5	101	119	3.1
55	158	4.4	149	166	2.9
30 (Ultrasone)	97	1.4	92	99	3.2

Table 3-I: *Channel depth measurement data (averages over all 30 measurement points).*

A distinct pattern is noticeable in these measurements: in general the middle channel of each chip is deeper than the bottom or top channel. Because the wafers were etched without any form of stirring or other convection promotion, a test was done to see if the uniformity improved when the wafer was ultrasonically agitated during etching. The results look promising: for 30 minutes etching, the average depth over the wafer was 97 nm, and the standard deviation was 1.4 nm (was 4.5 nm for 36 minutes etching without agitation). The etch rate of the ultrasonically etched wafer is a little higher than that of the wafers etched without agitation, probably because the OPD 4262 etchant heated up during the etching as a result of

the ultrasonic agitation. Alternatively, the agitation might enhance the removal of hydrogen gas which is produced during etching and could act as a mask.

The depth variation along the length of the channels was also measured by Dektak, but was found to be negligible.

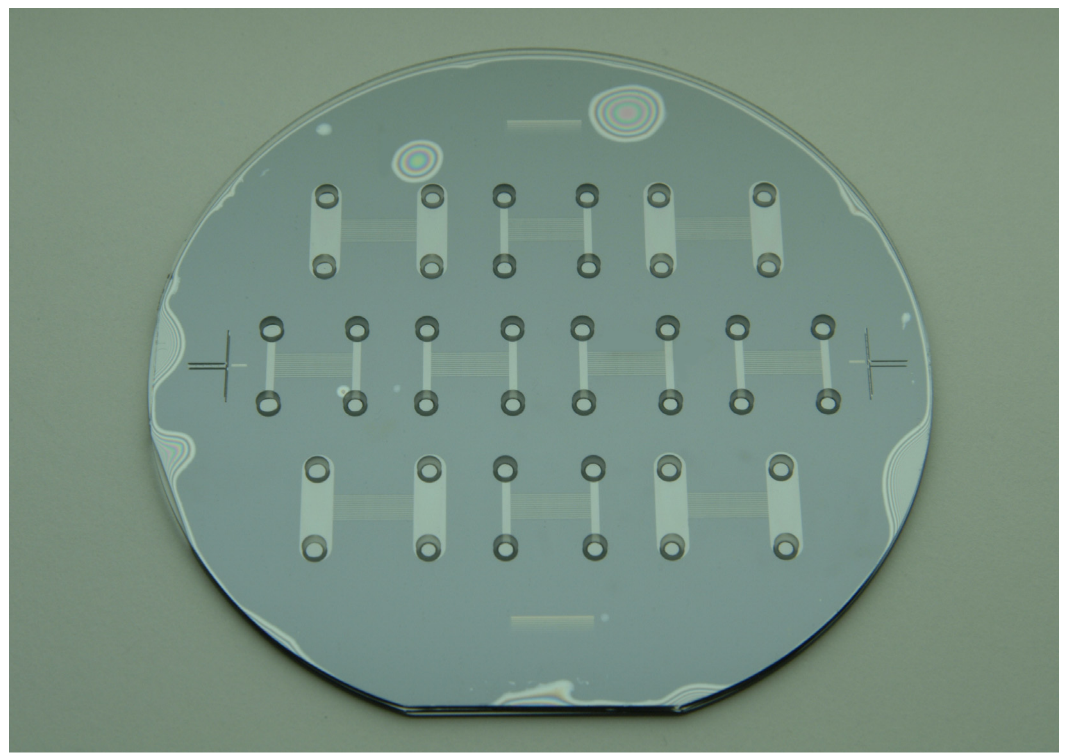


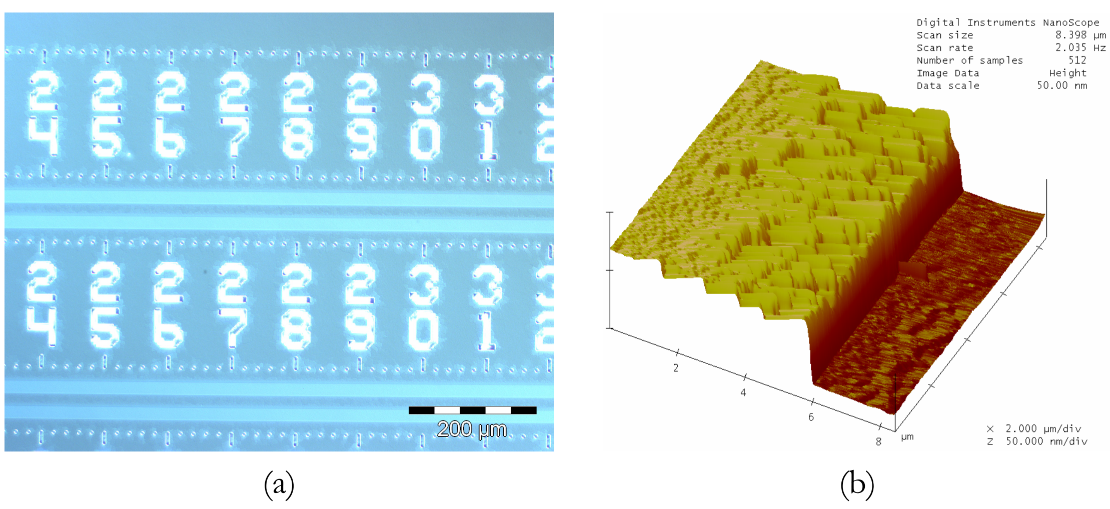
Figure 3-6: *100 mm wafer containing 10 chips with arrays of nanochannels: the powder-blasted access holes and the microchannels are clearly visible, as well as the alignment marks on the total left and right.*

The silicon to Borofloat bonding yielded an almost complete prebond by manually pressing the wafers together, and after the anneal step the bond looks even better (see Figure 3-6). The visible defects in the bond are caused by trapped particles on the interface between the two wafers: almost all other enclosures of air could be removed by "pushing" the voids in the direction of the chips, so the excess of air could be "ventilated".

3.3 Fabrication of chips using a dry oxide spacer layer

For the fabrication of chips with channel depths ranging from 5 to 50 nm, the previously described dry oxidation/(B)HF etching process was used (see paragraph

2.2). Two series of chips were fabricated: the first using BHF as the etchant, the second using 1% HF. The reason for the initial use of BHF for the etching of the channels, even though the overetch effect occurred, was that the adhesion of the photoresist to the Si substrate was initially insufficient to withstand the etching of a 50 nm thick layer of dry oxide in 1% HF: see Figure 3-7.



(a) (b)

Figure 3-7: *pictures of 50 nm deep channels etched using liquid HMDS priming and 1% HF. (a) Optical microscopic picture. (b) AFM 3D view of a step: the roughness due to delaminating can clearly be seen.*

Because BHF is less aggressive to the photoresist adhesion promoter, it was chosen as the initial etchant. With the arrival of a new HMDS priming system (low pressure vapor priming at a temperature of 150ºC, instead of liquid phase priming), it became possible to use 1% HF as a dry oxide etchant even for layers with a thickness of 50 nm.

3.3.1 Fabrication procedure

On the whole, the fabrication procedure, as shown in Figure 3-8 is similar to the wet anisotropic etching procedure. The main difference is that instead of the native oxide, a pre-grown dry oxide layer is patterned, and no additional silicon etch step follows (because the patterned dry oxide layer defines the height of the nanochannels after bonding). In addition the 20 nm thick dry oxide layer (which was grown to ensure that the channels etched using OPD 4262 were totally hydrophilic) is not grown in this process. This was done to ensure an accurate stepheight in the sub-10 nm range. An important result of this difference will become clear in the next chapter.

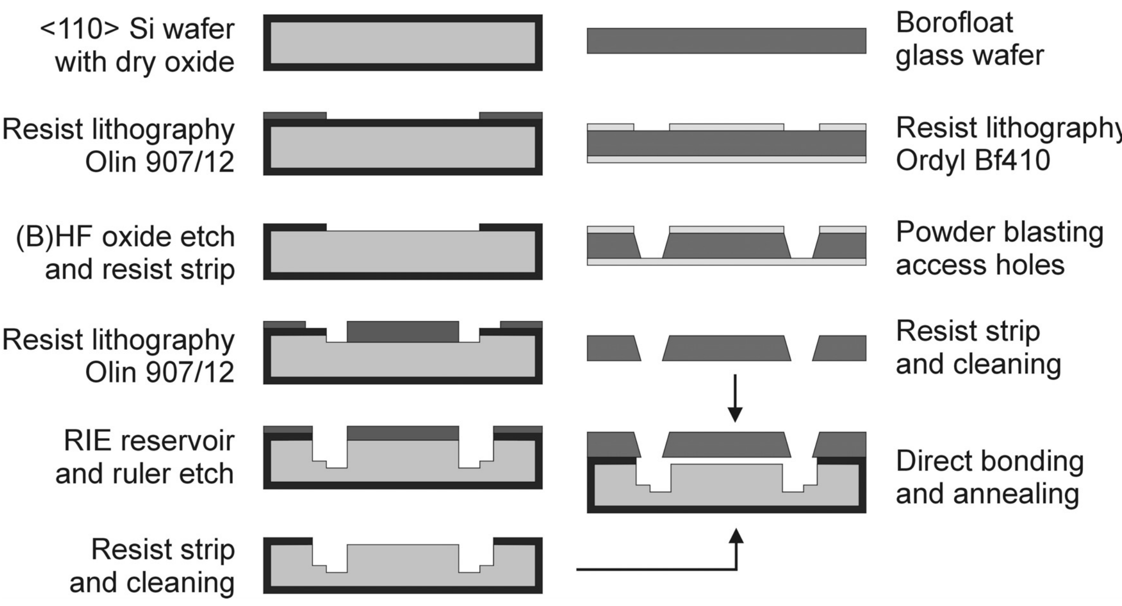


Figure 3-8: *Fabrication process for creating nanochannel chips, using a dry oxide spacer layer.*

The nanochannels were fabricated by bond nanomachining: a silicon <110> wafer was dry oxidized at 950ºC. The intended thicknesses of 6, 12, 25 and 50 nm required oxidation times of 1 min. 15 sec., 5 min. 30 sec., 22 min. 30 sec. and 75 min., respectively. After oxidation the oxide layer thickness was measured by ellipsometry, using a Plasmos SD 2002 ellipsometer (λ = 632.8 nm), and verified by a multi-wavelength Woollam M-44 NIR ellipsometer (λ = 600-1100 nm, in 44 steps). The measurements by the two different machines were always within 0.5 nm of each other, indicating a good ellipsometer measurement. For the actual measurement of the channel height the Plasmos ellipsometer was used, because it has the ability to do measurements at specific coordinates (i.e. the position of the channel on the wafer). For all wafers the Plasmos ellipsometer was used to create a raster pattern scan over the whole wafer, to check the uniformity of the layer. Also, at the position of each chip on the wafers, an oxide thickness measurement was done, so that later the channel height can be calculated for each chip individually.
After characterization of the oxide layer, the wafers were coated with Olin 907/12 photoresist, followed by exposure using the mask containing the nanochannels, and development. After developing, the resist received a hard bake (30 minutes at 120°C), followed by the etching of the channels in BHF (90 s) or 1% HF (with a visual etch stop: the etched wafer becomes hydrophobic when the oxide layer is completely etched). The resist was then stripped in fuming HNO_3 and a new

lithography step was done, using the reservoir/ruler mask. This pattern was then transferred into the silicon wafer by reactive ion etching on an Oxford Plasmalab 100 machine, to create the inlet/outlet reservoirs with a depth of approximately 20 µm. After resist stripping the wafers were standard cleaned and Piranha cleaned, together with the Borofloat cover-wafers, which have powder blasted [2] holes in order to provide access to the inlet/outlet reservoirs. After spin-drying the two wafers were fusion bonded, followed by an anneal step (4 hours @ 400°C).

3.3.2 Fabrication results

The oxide layers were characterized by ellipsometry: raster scans of four of the oxide layers can be found in Figure 3-9: these illustrate the uniformity of the layers.

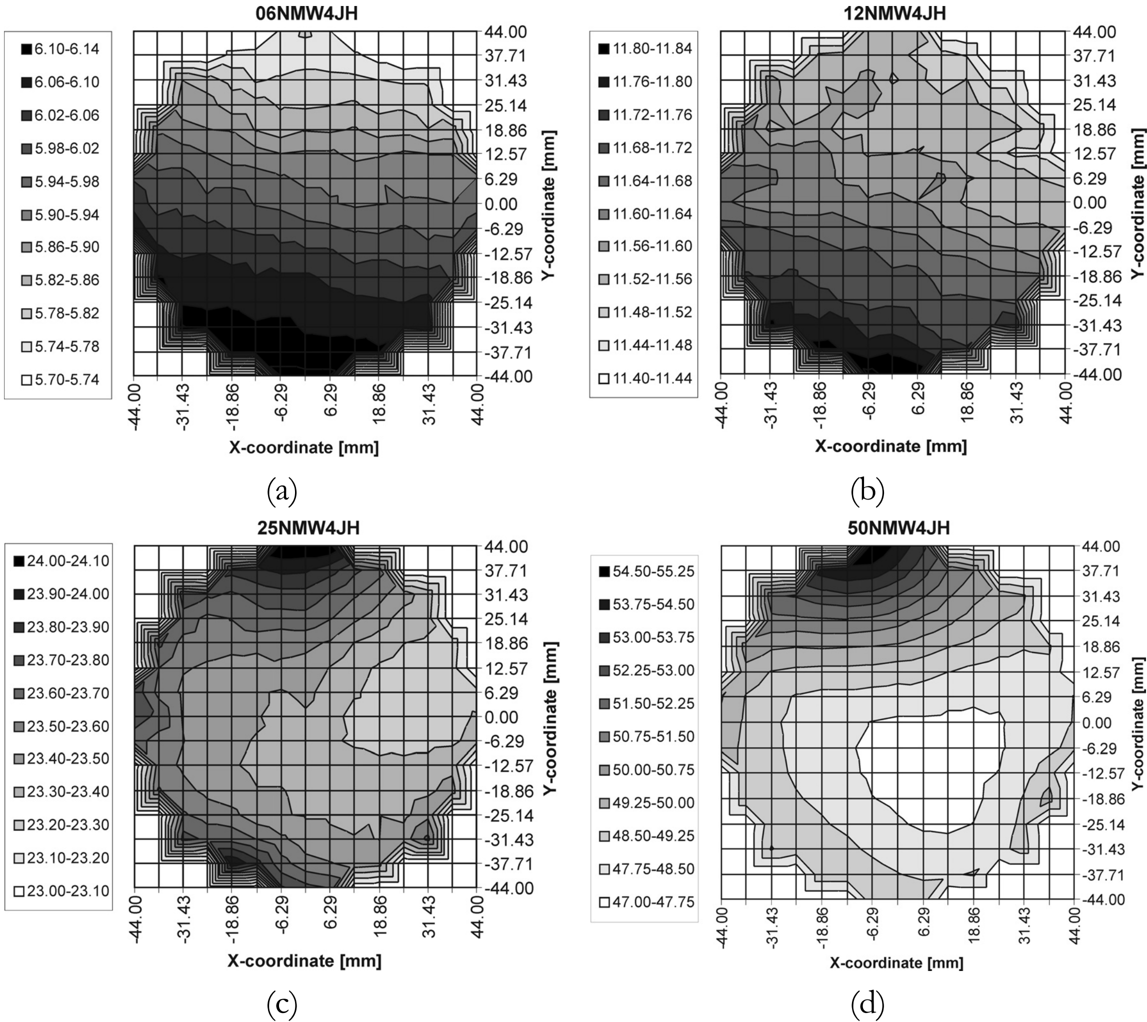


Figure 3-9: *Ellipsometer raster scans of SiO_2 layers with intended thicknesses of: (a) 6 nm. (b) 12 nm. (c) 25 nm. (d) 50 nm. The legends show the layer thickness in nm.*

The uniformity of the layers up to 25 nm is good: within 1 nm (± 2%) over the whole wafer surface. The 50 nm layer is somewhat less uniform, although the variation of the thickness over the area where the chips are positioned, is small (within 3 nm, i.e. ± 3%).

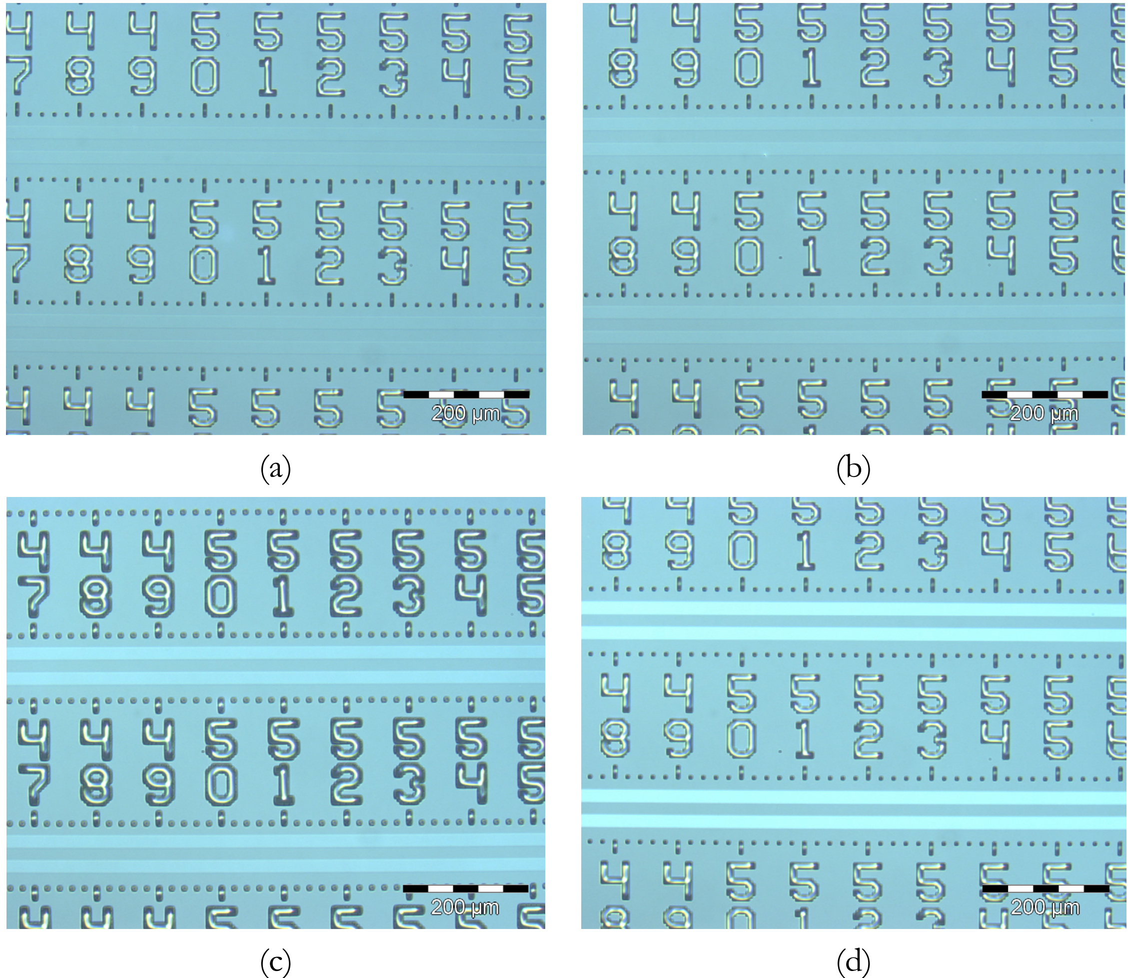


Figure 3-10: *Optical microscope pictures of etched wafers with oxide thicknesses of: (a) 6 nm. (b) 12 nm. (c) 25 nm. (d) 50 nm.*

After etching the nanochannels in (B)HF and the rulers with RIE, the chips are checked using optical microscopy (Figure 3-10). Interference-contrast microscopy enables the visualization of channels in oxide layers as thin as 6 nm (Figure 3-10(a)). The final channel heights of the finished chips were measured by means of ellipsometry and they were checked by AFM measurements. For the filling experiments, which will be performed in the next chapter, it is crucial that the height of the channels is determined accurately.

1% HF etched chips

The channel height calculation for the 1% HF etching process is explained in Figure 3-11: the final channel height can be calculated based on the ellipsometric measurements of the initial SiO_2 thickness and the native oxide after processing.

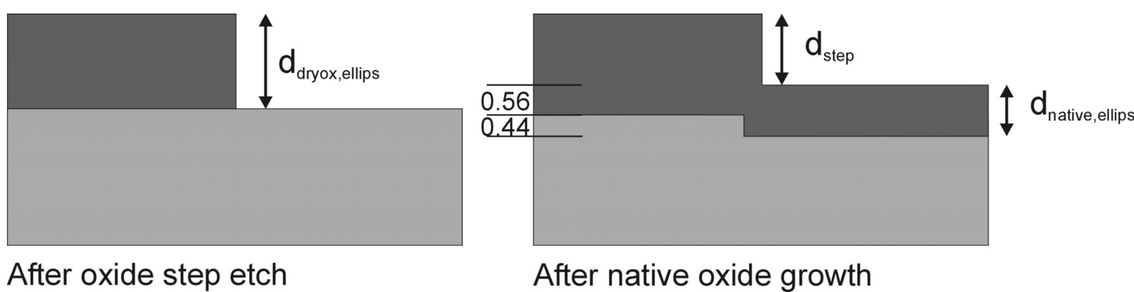


Figure 3-11: *Channel depth measurement/calculation for etching with 1% HF.*

The calculated channel height is given by equation (3.1).

$$d_{step} = d_{dryox,ellips} - 0.56 \times d_{native,ellips} \tag{3.1}$$

The native oxide thickness, as measured with the ellipsometer after annealing (on a dummy wafer), was 1.9 nm: so the effective channel depth decreases due to the growth of this native oxide layer is 0.56 · 1.9 = 1.1 nm.

Wafer #	Ellipsometer measurements			AFM
	$d_{dryox,\ ellips}$ [nm]	$d_{native,\ ellips}$ [nm]	Calculated d_{step} [nm]	Chan. depth [nm]
06nm	6.1 ± 0.5	1.9 ± 0.5	5.0 ± 0.8	5.1 ± 0.5
12nm	11.6 ± 0.5	1.9 ± 0.5	10.5 ± 0.8	11 ± 1
25nm	23.4 ± 0.5	1.9 ± 0.5	22.4 ± 0.8	25 ± 3
50nm	47.4 ± 1	1.9 ± 0.5	46.3 ± 1.3	52 ± 5

Table 3-II: *Channel depth calculation for 1% HF etched channels. The last column contains AFM measurements of the channels after processing.*

Table 3-II contains the ellipsometer measurements, as well as the corresponding AFM measurements, which were performed on the chips etched in 1% HF. The

data correspond well within the experimental errors. For these measurements the AFM was calibrated using a sample with $SrTiO_3$ steps: these steps are 0.39 nm each.

BHF etched chips

If the BHF etching method is used instead of 1% HF, the channel height measurement for the chips becomes more complicated (Figure 3-12): the value calculated by equation (3.1) has to be corrected by the "BHF overetch depth": i.e. the extra step that occurs because of the overetch in BHF (all chips were etched for a period of 90 seconds irrespective of oxide thickness, and the etch rate of thermal SiO_2 in BHF is approximately 70 nm/min).

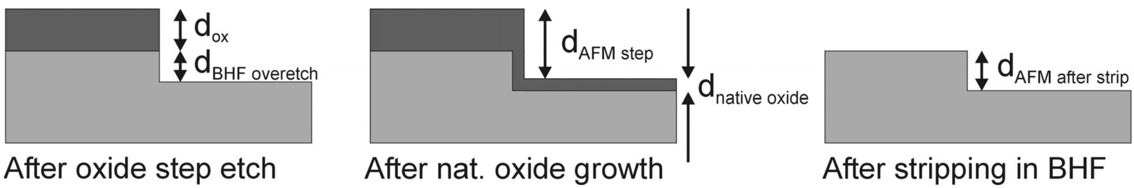


Figure 3-12: *Channel depth measurement/calculation for etching with BHF.*

For clarity the equations used to calculate the BHF channel height are repeated:

$$d_{AFM\ after\ strip} = d_{BHF\ overetch} + 0.44 \cdot d_{native\ oxide} \tag{3.2}$$

$$d_{ox,\ AFM} + d_{BHF\ overetch} = d_{AFM\ step} + 0.56 \cdot d_{native\ oxide} \tag{3.3}$$

The channel height d_{step} can be calculated by:

$$d_{step} = d_{ox,\ ellips} - 0.56 \times d_{native\ oxide,\ ellips} + d_{BHF\ overetch} \tag{3.4}$$

In these equations, the subscript "*ellips*" indicated a value measured by ellipsometry, instead of AFM. The actual formula which can be used to calculate the channel depth is found by substituting $d_{BHF\ overetch}$ from (3.2) into (3.4), giving:

$$d_{step} = d_{ox,\ ellips} + d_{AFM\ after\ strip} - d_{native\ oxide,\ ellips} \tag{3.5}$$

The reason that ellipsometry is still used as the dominant channel height measurement method instead of AFM, will be explained: the measurement error in

the ellipsometric measurement is ± 0.5 nm for SiO_2 layers with a thickness under 40 nm, and ± 1 nm for SiO_2 layers with a thickness over 40 nm (because in that regime the refractive index is not fixed, but is calculated based on the measurement data). On the other hand, the AFM measurements have an experimental error of ± 10% (the calibration of the AFM was again checked with a sample containing monosteps of $SrTiO_3$).

After stripping the dummy wafers in BHF and measuring of the resulting step height after the stripping, the step height on each of the channels was calculated using (3.5) and the ellipsometrically determined native oxide thickness. As an example, Table 3-III shows the calculations for chip #2 on each of the dummy wafers (only the AFM step measurement after stripping was done on chip #4).

Dummy Wafer #	$d_{AFM\ after\ strip}$ **[nm]** *(measured)*	$d_{native\ oxide,\ ellips}$ **[nm]** *(measured)*	$d_{BHF\ overetch}$ **[nm]** *(calculated)*	$d_{ox,\ ellips}$ **[nm]** *(measured)*	d_{step} **[nm]** *(calculated)*	$d_{AFM\ step}$ **[nm]** *(measured)*
06nm	4.0 ± 0.4	2.2 ± 0.5	3.0 ± 0.6	6.1 ± 0.5	7.9 ± 1.4	9.0 ± 0.9
12nm	4.4 ± 0.4	2.2 ± 0.5	3.5 ± 0.6	11.8 ± 0.5	14.0 ± 1.4	15 ± 2
25nm	3.9 ± 0.4	2.2 ± 0.5	3.0 ± 0.6	23.7 ± 0.5	25.4 ± 1.4	27 ± 3
50nm	3.4 ± 0.3	2.2 ± 0.5	2.5 ± 0.5	47.9 ± 1	49.1 ± 1.8	52 ± 5

Table 3-III: *Channel depth calculation for BHF etched channels. The last column contains AFM measurements of the channels depth after processing.*

From Table 3-III, it is concluded that the calculated channel heights correspond well with the AFM-based measurements in the last column.

Note that in reality the "$d_{AFM\ after\ strip}$" value might be influenced by the stripping itself: the BHF overetch amount might be overestimated, because in the stripping step the silicon on the bottom of the channel is exposed to the BHF earlier than the silicon at the top of the channel (it is only protected by a very thin layer of native oxide, while the silicon at the top is protected by a thicker dry oxide layer). However, this effect should be almost negligible for the 6, and 12 nm thick layers, because they are already removed after 5 and 10 seconds, respectively, after which both the bottom and the top silicon are exposed to BHF. Furthermore, if this effect would be very strong, the 25 and the 50 nm layers would have to show a step height

after stripping which is relatively higher than the values for 6 and 12 nm, and this is not the case. All in all, the BHF stripping is not expected to have a large influence on the channel height measurement, although with the gained knowledge it might have been preferable to use 1% HF for the stripping of the oxide layers.

3.4 Conclusions

Nanochannel chips (with 1D nanochannels, measurements rulers, and fluidic reservoirs) have been fabricated from a silicon wafer and a Borofloat cover wafer containing powder blasted fluidic access holes.

Chips containing channels with a depth in the order of 50, 100 and 150 nm have been produced using wet anisotropic etching of silicon (by OPD 4262 developer). The etch depth across the wafer showed larger variations than observed in the previous chapter: deviations up to ± 10% in channel depth were observed compared to the mean channel depth. However, when using ultrasonic agitation of the etchant during etching, the etch depth uniformity improved to ± 5% on a wafer with an average channel depth of 97 nm. No variations in channel depth along the length of a single nanochannel were observed.
Chips with smaller channel depths (ranging from 50 nm, down to 5 nm) have been produced in a well controlled manner by first growing a dry oxide spacer layer, followed by selectively etching of this layer in hydrofluoric acid. Channel depth variation across the chips on a wafer was measured to be less than ± 3%, for channel heights up to 50 nm. For optimum control over channel depth, 1% HF should be used to etch the SiO_2 spacer layer.

The chips are ready for filling with various liquids, which will be done in the next chapter.

3.5 References

[1] J. Haneveld, H. Jansen, E. Berenschot, N. Tas, and M. Elwenspoek, "Wet anisotropic etching for fluidic 1D nanochannels," *Journal of Micromechanics and Microengineering*, vol. 13, pp. 62-66, 2003.
[2] H. Wensink, "Fabrication of Microstructures by Powder Blasting," Ph.D. Thesis, University of Twente, Enschede, 2002.

4

Modeling and filling experiments*

In this chapter, a model for the capillary filling of the fabricated nanochannels is proposed. Capillary filling experiments with liquids such as water, NaCl solution and cyclohexane will be performed, and the results will be compared to the model.

* Based on: N. R. Tas, J. Haneveld, H.V. Jansen, M. Elwenspoek, and A. van den Berg, "Capillary filling speed of water in nanochannels," *Applied Physics Letters*, vol. 85, pp. 3274-3276, 2004, and: J. Haneveld, N. R. Tas, H.V. Jansen, M. Elwenspoek, "Accurate fabrication and characterization of sub-10 nm nanochannels", *to be submitted to Nano Letters.*

4.1 Introduction

Little is known about the behavior of liquid in channels with at least one dimension below 100 nm. One obvious property of nanochannels is that capillary forces are very prominent, due to the large surface to volume ratio. The wetting properties of the liquid in contact with the channel walls therefore play a crucial role in the filling process of nanochannels.

For carbon nanotubes this has been investigated by Dujardin et al. [1] who showed that they can be filled by low surface tension substances such as liquid sulfur, selenium and cesium. Ajayan and Lijima showed capillarity induced filling of carbon nanotubes by molten lead [2]. Multi-wall closed carbon nanotubes produced using a hydrothermal method were shown to contain a multiphase aqueous fluid [3]. Excellent wettability of the graphitic inner tube walls by the aqueous liquid was observed.

Sobolev et al. [4] measured the capillary pressure of water in quartz capillaries with radii ranging from 200 down to 40 nm, and showed that the Young–Laplace equation is still valid on the 100 nm length scale and that the surface tension of water on this scale is equal to the macroscopic value.

In this chapter we present the results of our measurements of the capillary filling speed of water in one-dimensional nanochannels with a height as low as 5 nm. These experiments are of practical value, because in nanofluidic experiments channels are usually filled by capillary action, and currently no accurate data is available about the filling speed. They are of fundamental importance because they may reveal if the viscosity of liquid in nano-confinement deviates from its bulk value, as has been suggested by Churaev et al. [5] and Hibara et al. [6].

4.2 Capillary filling model

In this chapter the capillary filling speed of micromachined rectangular nanochannels is modeled and measured. This was done for channels with a length of 1 cm, a width of 20 μm, and different heights between 5 and 150 nm. Similar measurements have been done on a larger scale (around 1 μm channel height) by

Yang et al. [7] and revealed that the filling speed can be described by the Washburn model [8], modified for the rectangular cross-section of the channel. Fully developed laminar flow is assumed (due to the low Reynolds numbers associated with the capillary filling of these channels). The Reynolds number *Re* describes the relative magnitude of inertia forces to viscous forces, and is defined as:

$$Re = \frac{\varrho v D_h}{\mu} \tag{4.1}$$

In this equation, ϱ is the density of the fluid [kg/m^3], v is the velocity [m/s], μ is the viscosity of the liquid [Pa·s], and D_h is the hydraulic diameter of the channel:

$$D_h = \frac{4A}{P} \tag{4.2}$$

Here, A is the cross-sectional area of the channel [m^2], and P is the perimeter length of the channel [m].

Liquid flow in circular pipes is expected to be laminar if Re<2300, above the value of 2300 the flow can be turbulent. For a channel with a diameter of 100 nm and water at room temperature as the liquid (ϱ = 1000 kg/m^3, μ = 0.001 Pa·s) and a velocity v = 0.006 m/s (this is a realistic value, observed in the first part of the channel during our filling experiments), this gives $Re = 6 \cdot 10^{-4}$. This easily falls in the laminar regime. It also means that for channels which are longer than their diameter, the flow will always be fully developed, because the entrance length is approximately given by [9]:

$$L_e = 0.06 Re D_h \tag{4.3}$$

The supply of liquid to the moving front can be modeled by a hydraulic resistance *R*, increasing proportional to the length x of the plug. For a rectangular channel, with a much larger width than the height, R becomes [10]:

$$\mathrm{R} = \frac{\Delta p}{\varphi_V} = \frac{12 x \mu}{w h^3}, \quad w \gg h \tag{4.4}$$

Here Δp is the pressure drop across the liquid plug [Pa], φ_V is the volume flow rate [m^3/s], w is the width [m], and h is the height of the channel [m]. The pressure drop Δp across the liquid column drives the liquid. It is equal to the capillary pressure p_{cap}, as the pressure at the channel entrance is equal to the atmospheric pressure p_0 and the pressure just behind the meniscus is equal to (p_0–p_{cap}): see Figure 4-1.

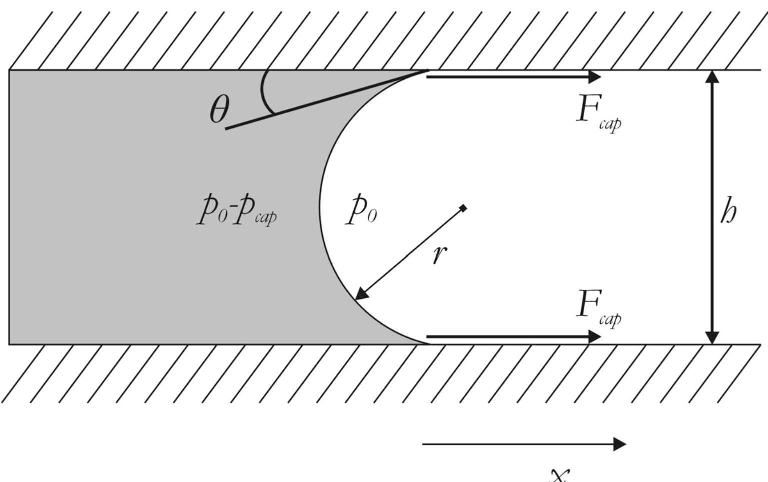


Figure 4-1: *Explanation of the capillary effect.*

The liquid/gas surface tension γ gives rise to a pressure drop Δp across the curved liquid/air meniscus. This is described by the Young-Laplace equation [11]:

$$\Delta p = \frac{\gamma}{r} \tag{4.5}$$

where r is the radius of curvature of the meniscus in the direction of the height of the channel; the radius of curvature in the width of the channel is neglected, because it is at least two orders of magnitude higher. The radius of curvature can be related to the channel height h and the contact angle θ by:

$$r = \frac{h}{2\cos\theta} \tag{4.6}$$

For a flat rectangular channel, the capillary pressure is then given by [12]:

$$\Delta p = p_{\text{cap}} = \frac{2\gamma\cos(\theta)}{h} \tag{4.7}$$

The volume flow φ_V is equal to the velocity of the moving meniscus (dx/dt) times the cross-sectional area (hw) of the channel. We can now derive the expression for the position of the moving meniscus as a function of time by combination of equations (4.4) and (4.7) and subsequent integration:

$$x = \sqrt{\frac{\gamma h \cos(\theta)}{3\mu}} \cdot \sqrt{t} \tag{4.8}$$

If the position of the meniscus during filling is measured, and plotted against the square root of the time, this should give a linear relationship if the modified Washburn equation is qualitatively valid.

4.3 Filling experiments using 150, 100 and 50 nm deep channels

4.3.1 Experimental data

The chips fabricated by the anisotropic wet etching process were used to study filling of the nanochannels by capillary force.

To measure the position of the meniscus as a function of time, a droplet of 7 μL demineralized (demi-) water (0.7 μS/cm, from a Millipore Elix3 water purification system) was introduced into the access holes in the glass by pipetting, and the entrance microchannel and nanochannels would fill by capillary action.

Digital video imaging with a frame rate of 25 images/s was used to record the filling process. For this, an upright microscope was used (Leica DM/LM), equipped with a Mitutoyo 10x LWD objective, M plan APO, NA = 0.28, in bright field mode. The recorded videos were analyzed frame by frame to measure the position of the meniscus as a function of time.

Figure 4-2: *A typical still image of the capillary filling of 110 nm deep channels (the large tick marks represent a distance of 100 μm).*

Figure 4-2 shows a typical still image from the video capture of the filling of 110 nm deep nanochannels. Starting at a certain critical length, bubbles tend to be formed at the liquid front, by enclosure of air. Measurements of the filling speed were carried out in the first part of the channels, up to the length where large bubbles start to form.

Figure 4-3 shows the measured position x of the moving meniscus as a function of $t^{1/2}$, for three channel heights (152 ± 11 nm, 111 ± 9 nm, 53 ± 6 nm). There is a near perfect linear relation between x and $t^{1/2}$, which means that there is excellent qualitative agreement with equation (4.8). The three curves are representative for all the measurements carried out. For each channel height, filling experiments were carried out four times with demi-water. For each experiment the slope a of the curve $x = at^{1/2}$ was determined and compared with the expected slope, based on equation (4.8), contact angle measurements, and handbook values for the viscosity and surface tension of water at the temperatures of the experiments [13].

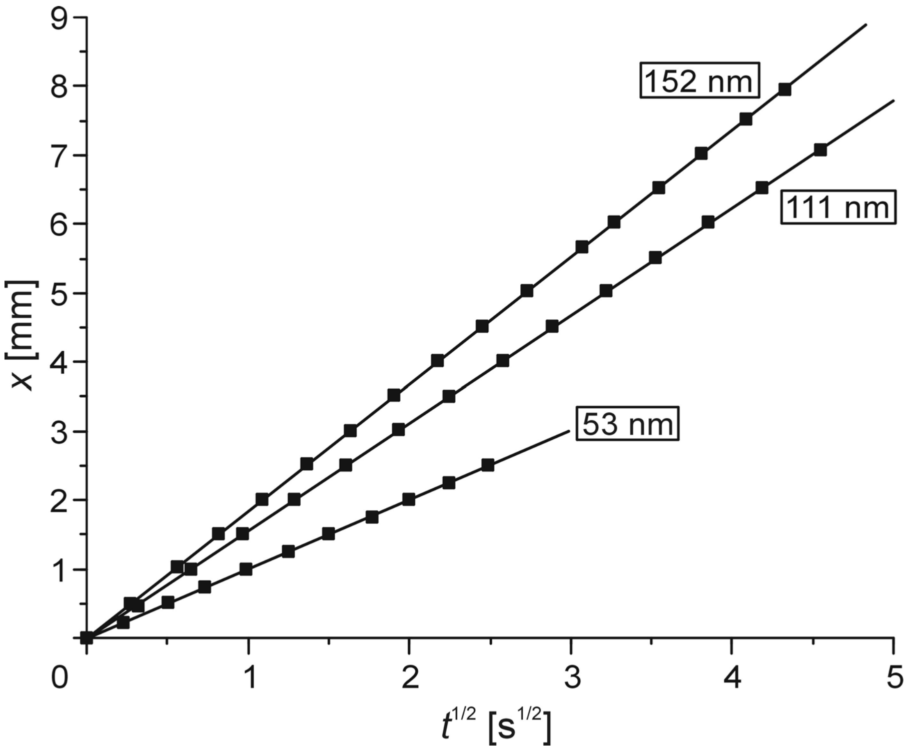


Figure 4-3: *Measured position x of the moving meniscus vs. the square root of the filling time, for three channel heights (152 ± 11 nm, 111 ± 9 nm, 53 ± 6 nm), and filling with DI water. These measurements were carried out at temperatures of 21.5, 21.9, and 22.0 ± 0.5°C, respectively. The error in the measured position is less than 20 µm, in $t^{1/2}$ it is less than 0.03 $s^{1/2}$. There is a near perfect linear relation between x and $t^{1/2}$; the R^2 value of the linear fits is larger than 0.9998.*

Contact angle measurement

Detailed knowledge of the contact angle is essential for a quantitative analysis of the filling experiments. For the water–silica system the picture is complex but can be well understood. For ultra low speed of the advancing contact line a thin adsorbed water layer is formed in front of the contact line, either by evaporation-condensation or by surface diffusion. Both advancing and receding contact line move over a "wet" surface and there is little or no contact hysteresis. For low speed of the contact line (typically in the range of 10 µm/s to 10 mm/s) there is no time for the adsorbed water layer to be formed, and the advancing contact line moves over a dry surface [14]. The receding contact line moves over a "wet" surface, as a thin water layer is left behind. This is the cause of the contact hysteresis in this regime. The contact hysteresis is independent of the velocity of the contact line. In the high speed regime (>>10 mm/s or Ca>>10^{-4}, where the capillary number Ca is given by $u\mu/\gamma$, with u the velocity of the contact line) the contact angle hysteresis

increases with increasing speed due to viscous losses near the moving contact line [15]. As experiments were carried out in the low speed regime (Ca = 10^{-5} - 10^{-4}), in the analysis we use the low speed advancing contact angle. The excellent $x = at^{1/2}$ behavior shows that this contact angle is indeed independent of velocity.

Because the materials and the surface treatment of the top surface and the bottom surface are slightly different, they also have different contact angles (θ_t and θ_b, respectively). Therefore, in equation (4.8) the following substitution has to be made:

$$\cos(\theta) = \frac{\cos(\theta_{a,t}) + \cos(\theta_{a,b})}{2} \tag{4.9}$$

The subscript "*a*" indicates that the advancing contact angle was used for the measurement. The contact angle on the Borofloat wafer ($\theta_{a,t}$) was measured on top of the glass cover wafer, at the same day as the filling experiments. At the same time, the contact angle for the bottom of the channel ($\theta_{a,b}$) was measured on a Si<110> dummy wafer, with 20 nm of dry thermal oxide (which received the same cleaning and annealing steps as the actual channels. This resulted in the value of 0.94 ± 0.02 in Table 4-I. All experiments were carried out at a relative humidity level of 20% - 40%.

Wafer	**θ_a [°]**	**cos(θ)**
Si <110> dummy + 20 nm SiO_2	27 ± 5	0.94 ± 0.02
Borofloat cover wafer	4 ± 1	

Table 4-I: *Contact angle measurements on top and bottom wafers.*

The differences in the measured and calculated slope are presented by the ratio of the apparent viscosity and the bulk viscosity of the liquid at the temperature of the measurements. This ratio is defined by the following equation:

$$\frac{\mu_{app}}{\mu_{bulk}} = \frac{\gamma h \cos(\theta)}{3\mu_{bulk} a^2_{measured}} \tag{4.10}$$

Figure 4-4 (diamonds) shows this ratio for the filling experiments with demi-water. The error bars represent the random errors, caused by the random errors in the channel height, the contact angle, and in the bulk viscosity as a result of the estimated error of the measured substrate temperature (± 0.5°C). The systematic error in the measured channel height (< 5%) is accounted for at the axes of the graph because it is the same for all measurement points.

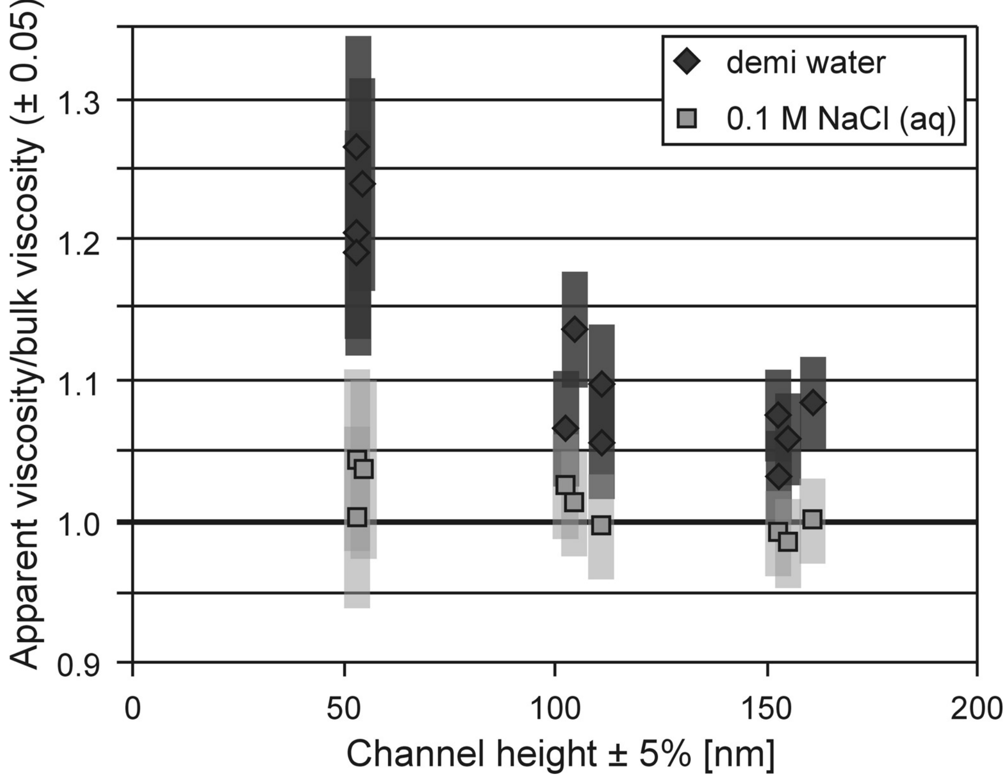


Figure 4-4: *Ratio of the experimentally determined apparent viscosity and the handbook values of the bulk viscosity, as a function of the channel height. Liquids used for filling were demi-water (diamonds) and a 0.1 M NaCl solution (squares).*

Figure 4-4 (in combination with the systematic error in the channel height measurement, accounted for at the axes) shows that for demi-water in the smallest channels the apparent viscosity is 23 ± 16% higher than the bulk viscosity, and that this number decreases to 7 ± 11% for the tallest channels. A possible explanation for this is the occurrence of the electro-viscous effect [16], which is an apparent increase of the viscosity due to electro-osmotic counter flow induced by a streaming potential. The electro-viscous effect is especially large under the condition of double layer overlap [16]. The demi-water experiments were carried

out in this regime. The demi-water used has a conductivity of 0.7 μS/cm at a pH of 5.8, which indicates that the main ionic content is H^+ and HCO_3^- from the dissociation of dissolved CO_2. For this content a Debye length of 0.2 μm can be estimated, as will be shown later.

To test the hypothesis further, the filling experiments were repeated in the same channels with a 0.1 M NaCl (aq) solution. Adding the salt significantly reduces the apparent viscosity to become close to the bulk viscosity (Figure 4-4, squares). This is consistent with the electro-viscous effect, because the high salt concentration strongly suppresses the streaming potential. Assuming that for the salt solution in the tallest channels the apparent viscosity is equal to the bulk viscosity, the systematic error in the measured channel height can then be eliminated, and for demi-water in the smallest channel the value of the apparent viscosity then becomes 24 ± 11% larger than the bulk viscosity, decreasing to 7 ± 6% in the tallest channels. Notion must be taken that the bulk viscosity increases when NaCl is added to the DI water. A 0.1 M NaCl solution has a bulk viscosity which is 1.0% higher than that of pure water, the surface tension is also increased, by 0.22% [17, 18]. We have corrected for these (small) changes in fluid properties.

Our results are in agreement with the findings of Churaev et al. [5], who found that the viscosity of water in glass capillaries of 80 nm diameter is approximately 40% elevated, and that this elevation decreases rapidly with increasing channel size [5]. Churaev et al. explained the elevated apparent viscosity by a possible increased ordering of the polar water molecules near the (negatively charged) channel walls. They estimated a thickness of 8 nm for the highly viscous boundary layer on the base of their experimental results. In our opinion this explanation is not satisfactory, because ordering of water near a charged surface is expected to occur only in the first few monolayers next to the surface [19-21], and therefore leads to a decrease in the effective channel diameter of approximately 2 nm or less. The electro-viscous effect is an attractive alternative explanation for the observed increase in apparent viscosity.

4.3.2 Electroviscous effects

Electroviscous effects are caused by the existence of an electrical double layer (EDL) and its influence on fluid flow in channels with dimensions in the order of the thickness of the double layer.

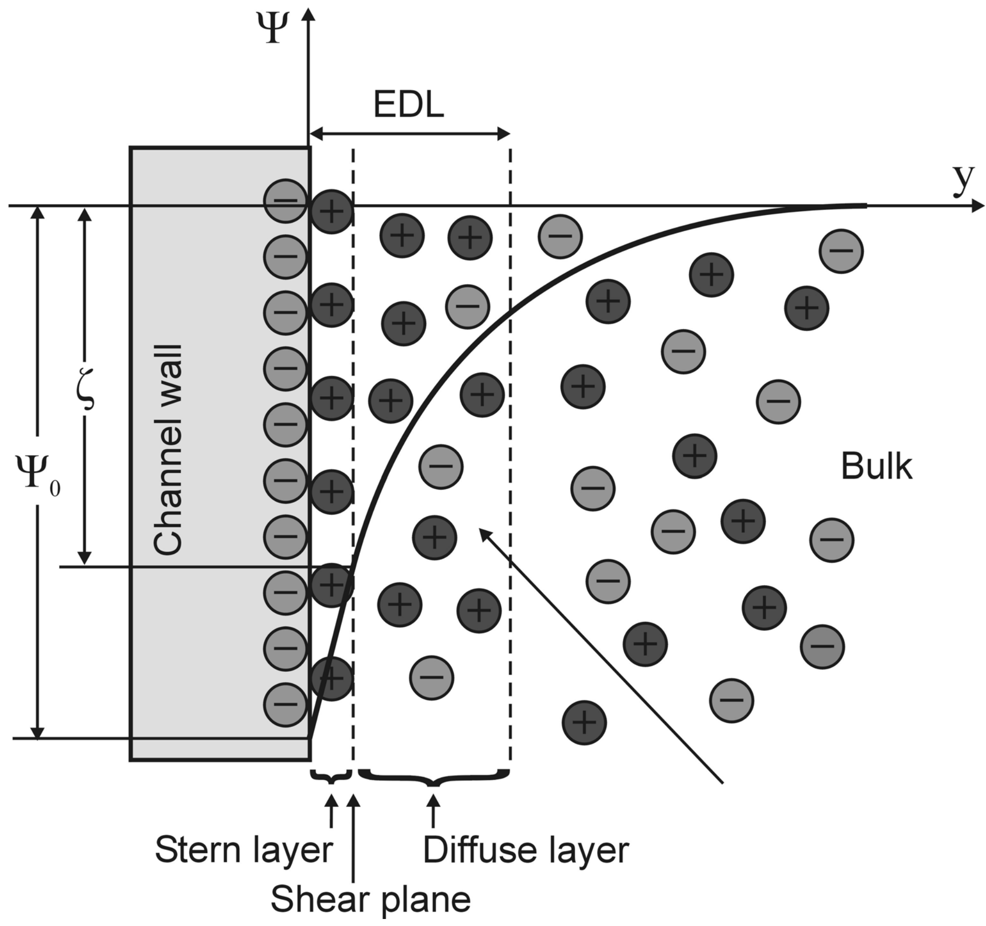


Figure 4-5: *Schematic representation of the electrical double layer (EDL) if the channel wall has a negative charge (as is the case in a SiO_2/H_2O system).*

In Figure 4-5, Ψ is the potential in the electrolyte, Ψ_0 is the surface potential, ζ is the zeta potential (the potential at the interface between the Stern layer and the diffuse layer), and y is the distance from the channel wall. When silicon dioxide comes into contact with water, the surface donates protons, leaving negatively charged SiO^- groups, which attract (positive) counterions from the electrolyte [22, 23]. Immediately next to the channel wall, there is a layer of immobilized ions (very strongly attached to the channel wall). This is called the immobile, or Stern layer. Next to the Stern layer, there is a region where the potential (and thus the

concentration of positive ions) decreases towards its bulk value. This region is called the diffuse layer (ions in this region are mobile).

In micro- and nanofluidics, three effects which are related to electrical charges are of importance: electrophoresis, electro-osmosis, and the streaming potential.

Electrophoresis
Electrophoresis is the transport of charged particles (ions) in a solution or suspension, under influence of an external electric field.
Electro-osmosis
The movement of a liquid caused by the drag that charges in the EDL exert on the surrounding liquid under influence of an electrical field.
Streaming potential
The electric field which is generated when a liquid is forced to flow past a stationary charged surface (this is in effect the inverse of the phenomenon seen in electro-osmosis).

So: if a fluid is forced through a channel with electrically charged channel walls, a streaming potential is generated because of the inhomogeneous distribution of ions in the channel (there is net charge transport due to the net charge in the mobile part of the EDL, which is carried downstream). This streaming potential will then cause a net back flow of the electrolyte (due to the electro-osmotic effect), thereby decreasing the net fluid flow in the forward direction. This decreased flow velocity can be expressed as an increase in the apparent viscosity of the fluid, as described in equation (4.10). The extent of this effect is largely dependent on the size of the channel, and on the ionic concentration of the liquid in the channel: the EDL layer thickness (also known as the Debye length) can vary between a few nanometers and microns, depending on the electrolyte concentration. In macrochannels, electroviscous effects generally have negligible influence. However, if the channel dimensions are of the same order as the EDL thickness, the increase in apparent viscosity can be substantial.

As mentioned above, the characteristic thickness of the EDL is called the Debye length, which can be calculated by taking the inverse of the Debye-Hückel parameter $\varkappa$:

$$\varkappa = \sqrt{\frac{e^2 \sum_i n_i z_i^2}{\varepsilon_0 \varepsilon_r k_b T}} \quad (4.11)$$

where n_i is the bulk ionic concentration of ion type i in the electrolyte, z_i is the valence of ion i, k_b is Boltzmann's constant ($1.38 \cdot 10^{-23}$ J K^{-1}), T is the temperature, e is the electron charge ($1.60 \cdot 10^{-19}$ C), ε_0 is the permittivity of free space ($8.85 \cdot 10^{-12}$ F m^{-1}), ε_r is the relative permittivity of the medium (80 for water). If we assume a symmetrical electrolyte with a valence of 1, the Debye-Hückel parameter becomes:

$$\varkappa = \sqrt{\frac{2e^2 n_0 N_A}{\varepsilon_0 \varepsilon_r k_b T}} \quad (4.12)$$

with n_0 the ionic molar concentration (mol m^{-3}) and N_A is Avogadro's constant ($6.02 \cdot 10^{23}$ mol^{-1})

The approximate ionic concentration of the DI water (needed to calculate the EDL thickness) can be calculated from the pH measurements and conductivity measurements, and equation (4.13) [24]:

$$\lambda = \sum_{i=1}^{k} n_i z_i u_i F \quad (4.13)$$

where λ is the total conductivity of the electrolyte, n_i, z_i, and u_i are the concentration, valence and mobility of ion i in the solution, and F is faraday's constant (equal to eN_A). If we assume that the main ionic species which are present in the electrolyte are H^+, HCO_3^-, Na^+ and Cl^-, then the H^+ concentration (which is the same as the HCO_3^- concentration) can be calculated from the pH measurement during the experiments (the pH value was measured to be 5.8). Then, using the measured value for the conductivity of the DI water which was used during the experiments ($\lambda = 70 \cdot 10^{-6}$ S/m), the concentration of NaCl can be calculated, after which

equation (4.11) can be used to calculate the Debye-Hückel parameter $\varkappa$ and the Debye length $1/\varkappa$. The measured and calculated values can be found in Table 4-II. In this table the values for the ionic concentration of the user made 0.1 M NaCl solution are set to 100 mol/m^3.

	Ion	**Ionic mobility [m^2/Vs]**	**Concentration [mol/m^3]**	**EDL thickness ($1/\varkappa$) [nm]**
DI water	H^+	$36.23 \cdot 10^{-8}$	$1.58 \cdot 10^{-3}$	$2 \cdot 10^{2}$
	HCO_3^-	$4.62 \cdot 10^{-8}$	$1.58 \cdot 10^{-3}$	
	Na^+	$5.19 \cdot 10^{-8}$	$0.56 \cdot 10^{-3}$	
	Cl^-	$7.91 \cdot 10^{-8}$	$0.56 \cdot 10^{-3}$	
0.1 M NaCl	Na^+	$(5.19 \cdot 10^{-8})$	100	1
	Cl^-	$(7.91 \cdot 10^{-8})$	100	

Table 4-II: *EDL thickness calculation for DI water and 0.1 M NaCl solution.*

It must be noted that it is only an assumption that the other species present in the DI water are Na^+ and Cl^-: in reality, there might well be other constituents in the electrolyte, adding to the conductivity. However, most ions have a mobility which is in the same range as that of Na^+ and Cl^- (H^+ is a real exception here, because of its very small size it has a very high mobility), so the calculated ionic concentration will also be in the same order, as will be the thickness of the EDL.

We have tried to compare the data from the experiments to theoretical models describing the dependence of the electroviscous effect [16, 25-27]. This proved to be very difficult because of a number of factors. The apparent viscosity increase depends strongly on the zeta potential and on the EDL thickness. The zeta potential is unknown for the current experiments, and the EDL thickness can be influenced by deprotonation of the channel walls. When the wall donates protons to the liquid during filling, the H^+ concentration can rise considerably [22, 23], and the EDL thickness is lowered. The lower pH also has an effect on the value of the zeta potential. Because the extent of the deprotonation effect is unknown, quantitative comparison to theory is difficult. Further experiments (zeta potential

measurements and channel wall deprotonation investigations) should be done to be able to enable quantitative comparisons to theory.

4.4 Filling experiments using 5, 11, 25 and 50 nm deep oxide spacer channels

For measuring the capillary filling dynamics of the oxide spacer layer chips, the channels were observed under an upright microscope (Leica LM/DM) in bright field mode for the 22 nm and 46 nm channels, and using Differential Interference Contrast (DIC) for the 11 nm and 5 nm channels. Mitutoyo 20x and 50x LWD objectives (M plan APO SL, NA = 0.28 and 0.42, respectively) were used. DIC microscopy proved to be a very valuable tool to study the behavior of liquids in nanochannels, making it possible to see even layers of liquid with a thickness of 5 nm. Therefore in the next paragraph a short introduction to this technique will be given.

4.4.1 Introduction in DIC microscopy

Since the contrast provided by bright field microscopy is very low when the channel depth is below 20 nm, for the filling of the 6 and 12 nm chips differential interference contrast (DIC) microscopy [28] was used to observe the fluid flow in the channels. This technique was developed by French optics theoretician Georges Nomarski [29]. He used a modified Wollaston prism (a Nomarski prism) in his microscope set-up. It consists of two birefringent prisms, which are cemented together, and have their crystal axes perpendicular to each other. The basic parts of a DIC microscope can be seen in Figure 4-6.

In the microscope, a linearly polarized beam of light is created by the polarizer. The first Wollaston prism splits it into two diverging beams perpendicularly polarized to each other: one “ordinary” O-wave, and one “extraordinary” E-wave. The condenser converts the angularly split rays into two parallel rays, separated by a distance d_{split} (which is smaller than the resolution of the optics). The two rays then pass through the specimen and the objective, and they are recombined in the second Wollaston prism. They pass the analyzer and interfere to give intensity differences, depending on the phase difference between the E- and the O-waves. In the figure, when the E- and the O-wave both have the same optical path length, the

intensity after the analyzer will be zero (the analyzer is 90 degrees turned with respect to the polarizer). If, however, there is a different path length (e.g. because of thickness variations in the sample, or a gradient in refractive index) the E- and the O-wave will be slightly out of phase. After the analyzer, interference of the two beams will then result in an intensity or color. The use of an initial phase offset between the E- and O-waves enables the generation of color contrast in the final image: see Figure 4-7.

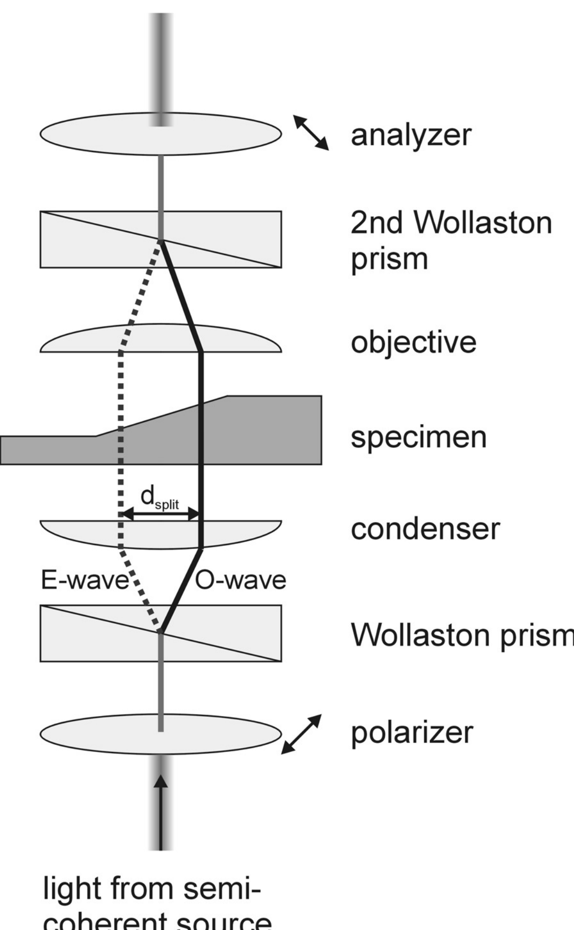


Figure 4-6: *Principle of operation of a differential interference contrast microscope.*

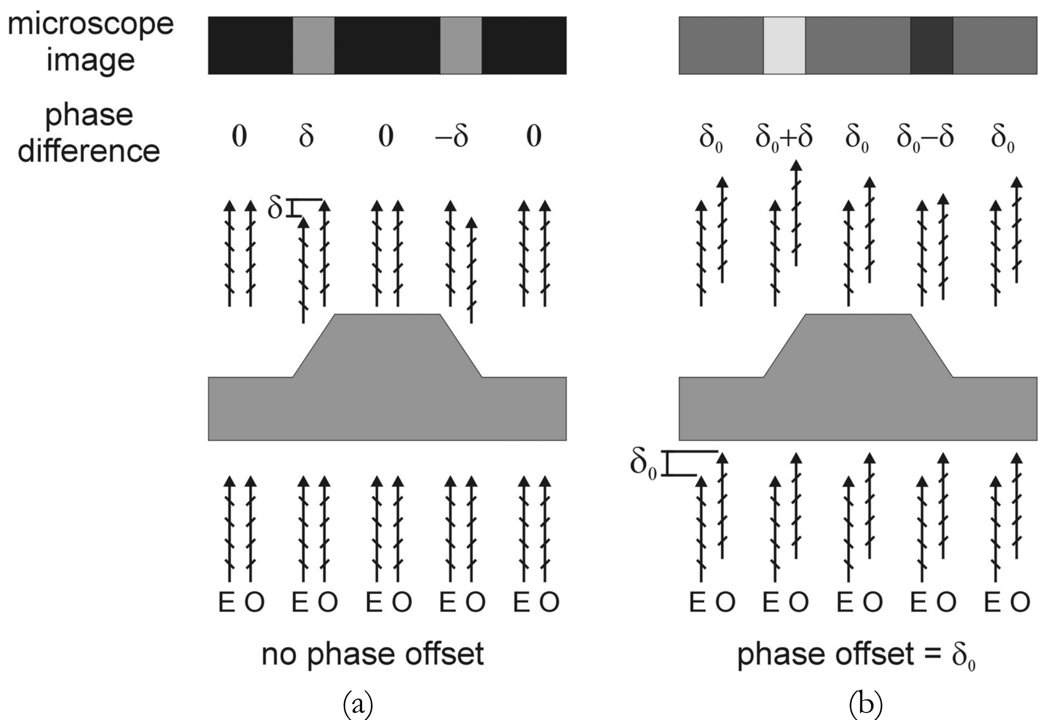


Figure 4-7: *Image generation using DI:,(a) with, (b) without initial phase offset (based on [28]).*

Even layers of water with a thickness of 5 nm generate enough contrast to be made visible using this technique: something that would be extremely difiicult using ordinary bright field microscopy.

4.4.2 Experimental data

Cyclohexane (Merck, pro-analysis ≥ 99.5%) and DI water were introduced into the access holes and would fill the chip by capillary action. The position of the moving meniscus as a function of time was recorded and could be accurately determined using the rulers next to the nanochannels. Cyclohexane was chosen for these experiments as it is expected to give little or no electroviscous effect [30] and because it is completely wetting on silica surfaces, which means the contact angle is fully determined ($\cos(\theta) = 1$). The contact angles of water were determined to be less than 5 degrees ($\cos(\theta) = 1$) on both a silicon dummy wafer and a Borofloat dummy wafer. Figure 4-8 shows a typical still-image of the filling experiment with cyclohexane in 11 nm channels. The position of the meniscus is at 1.5 mm. Using DIC it is possible to observe the moving meniscus down to even 5 nm channel height, although at this height the contrast becomes very low.

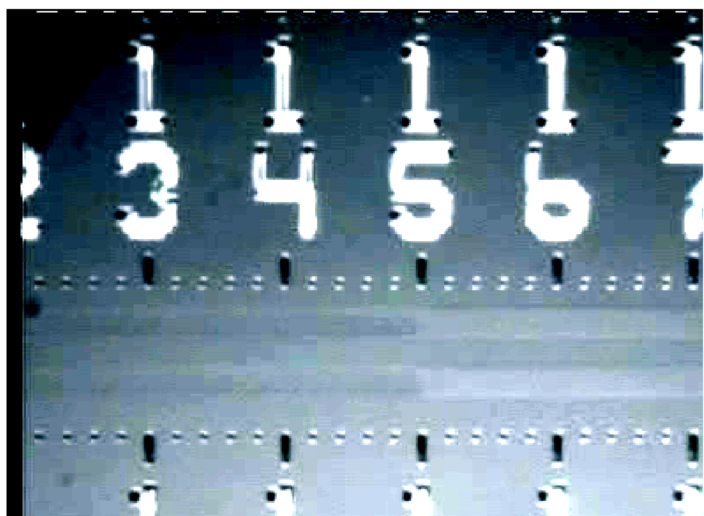


Figure 4-8: *Typical still image of the filling experiment of the 11 nm channels. The meniscus is located around 1.5 mm. The contrast has been slightly increased compared to the original DIC image.*

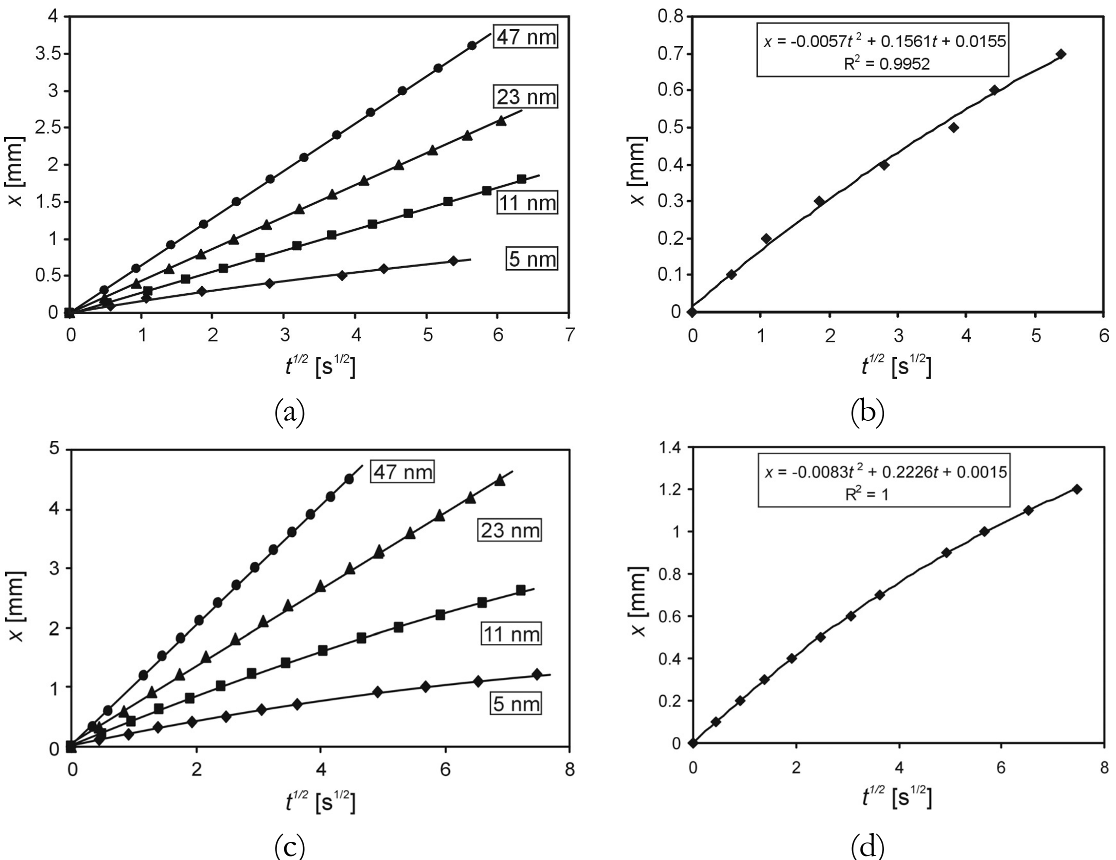
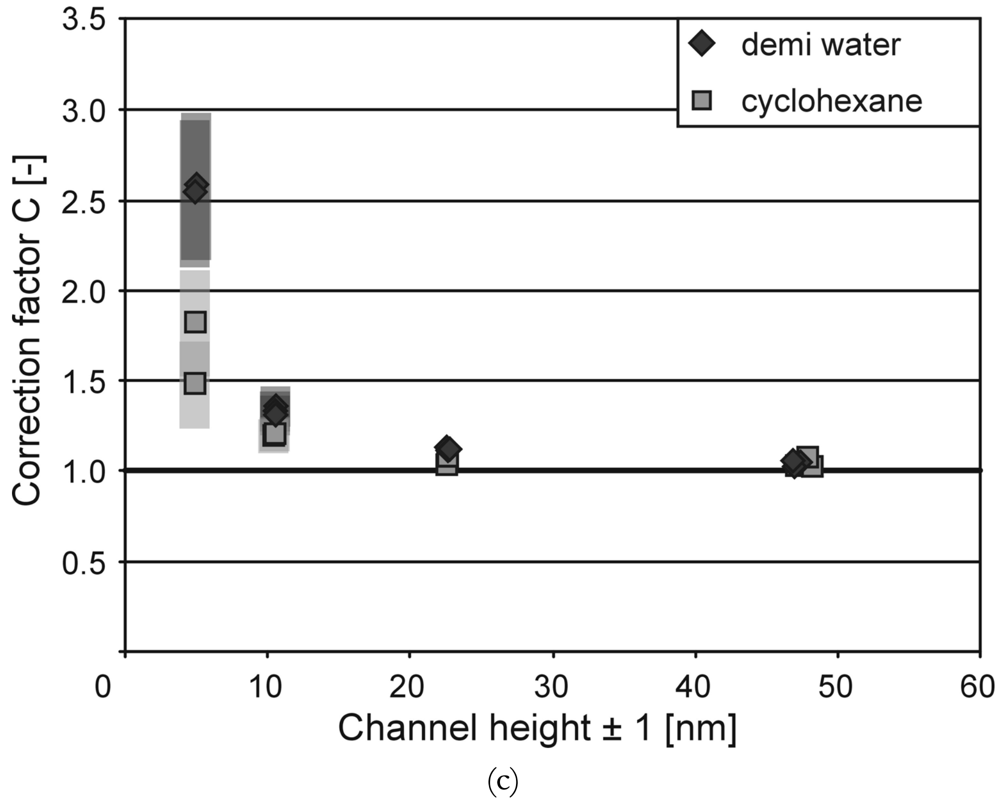


Figure 4-9: *(a) Measured position of the moving meniscus as a function of $t^{1/2}$ for filling of 5, 11, 23 and 47 nm deep channels with cyclohexane (at temperatures of 22.9, 22.4, 22.0 and 21.2 ± 0.5 °C, respectively). (b) Detailed representation of the graph for the 5 nm deep channel. (c)/(d) The same, but for filling with DI water (at temperatures of 22.7, 22.2 21.6 and 20.8 °C for the 5, 11 23 and 47 nm deep channels, respectively).*



(c)

Figure 4-10: *The measured correction factor C for filling with cyclohexane and DI water. The deviation from the calculated value increases gradually for smaller channel heights and reaches 1.6 ± 0.4, and 2.6 ± 0.4 for the 5 nm channels for filling with cyclohexane and water, respectively.*

Figure 4-9(a)/(c) show the measured position of the moving meniscus as a function time, for all four channel heights, and filling with cyclohexane and water, respectively. The filling is again expected to follow the classical Washburn equation (equation (4.8)). Therefore, in Figure 4-9(a)/(c) the position of the meniscus is plotted as a function of $t^{1/2}$, and a straight line is expected. However, there is a small deviation from the expected Washburn behavior (see Figure 4-9(b)/(d)), which can be accounted for by a constant loss of liquid per unit time at the (moving) meniscus. This loss could for instance be caused by corner flow, or evaporation of liquid at the meniscus. The drawn lines in Figure 4-9(b)/(d) are fits including this term, which is linear in t. For filling of the 5 nm deep channels with cyclohexane this correction term corresponds with a constant speed reduction of 6 μm/s (for water this linear term was determined to be approximately 8 μm/s).

Corrected for this effect, the filling dynamics is described by $x = a \cdot t^{1/2}$, and the measured value $a_{measured}$ was compared to the calculated value $a_{calculated}$ by a correction factor C, as shown in equation (4.14). The factor C has the same form as the relative apparent viscosity in equation (4.10).

$$\sqrt{C} = \frac{a_{calculated}}{a_{measured}} = \frac{\sqrt{\frac{\gamma h \cos(\theta)}{3\mu}}}{a_{measured}} = \sqrt{\frac{\gamma h \cos(\theta)}{3\mu a_{measured}^2}} \tag{4.14}$$

Figure 4-10 shows the correction factor C for the four different channel heights and the two different liquids. As can be seen from this figure, the deviation from the model value of a gradually increases for smaller channel heights and is significantly higher than unity (1.6 ± 0.4 for cyclohexane, and 2.6 ± 0.4 for water) for the 5 nm channels. The reason why we do not speak of a rise in the apparent viscosity of the liquids is that it is unsure which phenomena cause the filling process to be slower than modeled. The factor C can include various effects, amongst which the electroviscous effect, ordering of molecules directly next to the channel walls, and geometrical effects are a few of the most likely candidates to explain the observed effects. They will be discussed below.

Electroviscous effects

When comparing the results for filling with DI water from the 47 nm deep channels in Figure 4-10 to those of the 53 nm deep channels in Figure 4-4, it seems at first surprising that the deviation from the model in Figure 4-10 is practically zero, while the channels are even a little smaller. The most likely explanation for this is that the chips fabricated with a dry oxide spacer layer are not electrically isolated from the bulk silicon by a dry oxide layer (as was the case for the results in Figure 4-4), but only by a very thin native oxide layer. The streaming current can now leak away through the bulk silicon, prohibiting the buildup of a streaming potential, and thereby eliminating the electroviscous effect.

When cyclohexane is used as the filling liquid, the electroviscous effect can not be responsible for a deviation from the calculated value of a.

Viscosity effects

Estimating the diameter of the volume which is occupied by one cyclohexane molecule to be 7 Å, the smallest channels have a height of approximately 7 molecules. Let us assume there is a less mobile layer of ordered liquid molecules next to the channel walls [31], which effectively decreases the channel height h. The results in Figure 4-10 are consistent with a cyclohexane layer of 0.7 nm (or approximately one monolayer) thick next to each wall. This would explain the observed deviation from the model.

In the case of water this interpretation would result in a highly viscous layer of 1.1 nm thick next to each wall. As the water molecules are smaller in diameter than the cyclohexane molecules, this leads to approximately 4 monolayers of water in this highly viscous boundary layer.

Geometry effects

Aside from the possible decrease in effective channel height by the ordering of liquid molecules adjacent to the channel walls, there is also the possibility of a physical decrease of the channel height, due to elastic deformation of the channel walls under the large negative pressures associated with capillary filling (i.e. an inverse indent) [32]. The pressure just behind the water meniscus is -29 bar at a channel height of 50 nm, and even as large as -290 bar for 5 nm deep channels. Simulations should be performed to see if the channel is significantly deformed under large negative pressures.

Surface roughness effects

Surface roughness on the bottom and the top of the channel is not expected to have a large influence on the channel resistance (and therefore the filling speed), because of the excellent surface roughness values observed during the nanochannels fabrication process. The channels had a roughness of 0.16 nm RMS on the bottom of the channel, and 0.22 nm RMS on the top (the Borofloat wafer).

4.5 Conclusions

Filling experiments have been performed using the fabricated chips. The silicon (OPD 4262 wet etched) channels were filled with DI water as well as a 0.1 M NaCl solution. When compared to a model based on the modified Washburn equation

for capillary filling, this model qualitatively describes the experiments very well: the position of the meniscus in the channel is proportional to the square root of the filling time. Quantitatively, the filling with DI water was slower than expected (expressed as an increase of the apparent viscosity of 24 ± 11% for the 53 nm deep channels, and 7 ± 6% for the 152 nm deep channels). The elevated apparent viscosity is attributed to the electroviscous effect. This is supported by the cancellation of the observed effect by the addition of 0.1 M NaCl to the water. No quantitative comparison of the observed electroviscous effect to theory could be made, due to the fact that the zeta potential and the extent of channel wall deprotonation are both unknown. Additional experiments should be done to investigate the mentioned effects.

The dry oxide spacer layer chips, etched with the 1% HF solution, were filled with cyclohexane and DI water. Quantitative deviations from the model up to a factor 2.6 ± 0.4 (water) and 1.6 ± 0.4 (cyclohexane) for the 5 nm deep channels were observed. This can not be satisfactorily explained by electroviscous effects. A number of alternative explanations was presented, including a less mobile layer of ordered liquid molecules adjacent to the channel wall which effectively decrease the channel height (by approximately 1.4 nm for cyclohexane and by approximately 2.2 nm for water). Another explanation could be that the channel walls get elastically deformed under the large negative pressures associated with capillary filling of these channels. Furthermore, an effect was observed which can be accounted for by a constant loss of liquid per unit time. This can be caused by for instance corner flow or evaporation of liquid from the moving meniscus during filling. In the smallest channels this amounted to an approximate filling speed reduction of 6 μm/s for cyclohexane and 8 μm/s for filling with water.

In the future, more experiments and simulations should be conducted to investigate the effects observed in this chapter more elaborately.

4.6 References

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5

2D nanochannel fabrication*

Having the channel depth under control down to the sub-10 nm range, the width of the channel can be reduced, to produce true 2D nanochannels. Since standard optical contact lithography techniques are limited to a resolution of approximately 1 micrometer, alternatives have to be developed.
Two possible technologies are proposed and described: laser interference lithography in combination with wet anisotropic etching of silicon, and the creation of nano-ridges by the local oxidation of silicon edges (contour lithography).

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* The paragraphs concerning the fabrication of nano-ridges are based on: J. Haneveld, E. Berenschot, P. Maury, and H. Jansen, "Nano-ridge fabrication by local oxidation of silicon edges with silicon nitride as a mask," *Proc. Micromechanics Europe Conference 2005*, Göteborg, Sweden, September 4-6, pp. 72-75, *submitted to Journal of Micromechanics and Microengineering*.

5.1 Nano-ridge fabrication by local oxidation of silicon edges with silicon nitride as a mask

Currently, several tools are available to create patterns having a width in the nanometer range. These patterns are useful as imprint stamps to define 2D nanostructures in e.g. a polymer layer [1]. In this way, one master mold can be used for fast and easy replication of large series of structures. People have used E-beam to write structures in PMMA [2], Focused Ion Beam (direct milling of the substrate) [3], or AFM writing techniques [4, 5]. However, these techniques have one main drawback in common: they are *writing* techniques. Wafer-scale writing of nanopatterns is a time (and thus money) consuming activity, if not impossible altogether.

A method to fabricate ridges with a width in the nanometer range, and variable height, is proposed here. The processing will be done using common optical photolithography and wet etching techniques. An additional feature of the proposed technique is the ability to double the density of lines when a periodical pattern is desired. This is an inherent property of so-called edge or contour lithography processes [6-8].

The process documentation used for the fabrication of the nano-ridges can be found in the Appendix.

5.1.1 Fabrication process

In the proposed process 100 mm, double side polished, p-type <110> silicon wafers (5 - 10 Ωcm) were used. After an introductory standard cleaning step (10 min fuming HNO_3, followed by 10 min boiling HNO_3) and native oxide removal in 1% HF, a very thin (8 - 15 nm) low stress LPCVD SiN_x silicon-rich nitride layer was deposited on the wafers, followed directly by deposition of a thin (40 - 100 nm) TEOS oxide layer (Figure 5-1(a)). Then, a layer of positive photoresist (Olin 907/12) was spin-coated and optically exposed using a mask containing 4 μm wide grating lines. The resist was developed using Olin OPD 4262. After a postbake of 30 minutes at 120°C, the resist line pattern was transferred to the TEOS layer by etching in 1% HF or BHF. The etch time was 60 s in BHF for

the 100 nm layer (etch rate ≈ 180 nm/min), or 150 s in 1% HF for the 40 nm layer (etch rate ≈ 33 nm/min). A visual etch stop was not possible, because the oxide layer and the underlying silicon nitride layer are both hydrophilic. For this reason, a rather generous overetch (approximately 100% in time) was applied to be sure to actually reach the nitride layer underneath.
After the pattern transfer into the TEOS layer, the photoresist was stripped in fuming nitric acid for 20 minutes, and the wafers received a standard HNO_3 cleaning step (Figure 5-1(b)).

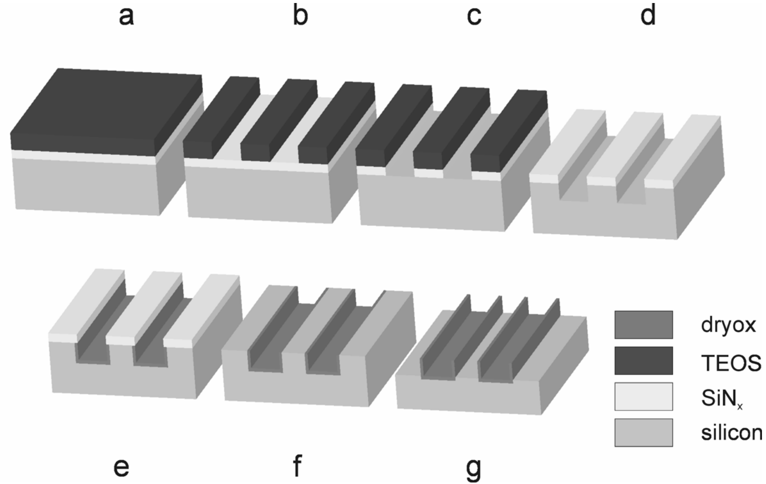


Figure 5-1: *Basic process flow for nano-ridges fabrication (notice the doubling of the spatial frequency of the lines).*

Subsequently, the TEOS oxide pattern was transferred to the silicon nitride layer by means of etching in hot phosphoric acid (85% H_3PO_4 @ 180°C) (Figure 5-1(c)). Then, the TEOS layer was stripped in BHF or 1% HF, directly followed by low speed wet anisotropic etching of the exposed <110> silicon areas in OPD 4262 developer [9]: Figure 5-1(d). The use of <110> silicon allowed for the etching of trenches with 90° sidewalls in the silicon wafer. The silicon etch step was followed by a standard cleaning step and a 1% HF dip (to remove the oxide that has been formed during the standard cleaning). Then the wafer was dry oxidized locally at a temperature of 950°C, with the nitride mask protecting the areas of the wafer that should not be oxidized (Figure 5-1(e)). After this so-called LOCOS process (LOCal Oxidation of Silicon [10-12]), the nitride mask was stripped in hot H_3PO_4 (Figure 5-1(f)), directly followed by another wet anisotropic silicon etch to etch back the now exposed silicon areas (Figure 5-1(g)).

The final result of the process in Figure 5-1 is a wafer-scale array of oxide ridges. The width of the ridges can be defined precisely by the thickness of the dry oxide layer (and therefore by the oxidation time). The height of the ridges can be accurately tuned by adjusting the OPD 4262 silicon etching time. As an inherent feature of the process, the period of the structures has been decreased from 1 line per 8 μm to 2 ridges per 8 μm. This period doubling feature was also used by Ribbing et al. to fabricate saw-tooth refractive x-ray lenses in <100> silicon [13].

5.1.2 Fabricated nano-ridge structures

In Figure 5-2, a nano-ridge of approximately 20 nm wide is shown. A difference (intentional) in the etching time between the two silicon wet etching steps led to a clear difference in height left and right of the ridge. In Figure 5-3, ridges of 15 and 7 nm wide can be seen. The two silicon etching steps were equally long in both figures (10 minutes each), leading to a height of the ridges of approximately 40 nm. An AFM scan of one of the fabricated structures can be found in Figure 5-4, proving the excellent uniformity. A slight level difference can be seen in the AFM scan. This is due to the fact that the oxidizing silicon surface was elevated during the dry oxidation step, or due to a small difference in etch time between both stages. The twisting of the oxide ridges, observed in Figure 5-3, was caused by imperfections in the mask used for optical lithography. The mask quality can be improved, but it is not an issue for the current study of the fabrication aspects of the stamps.

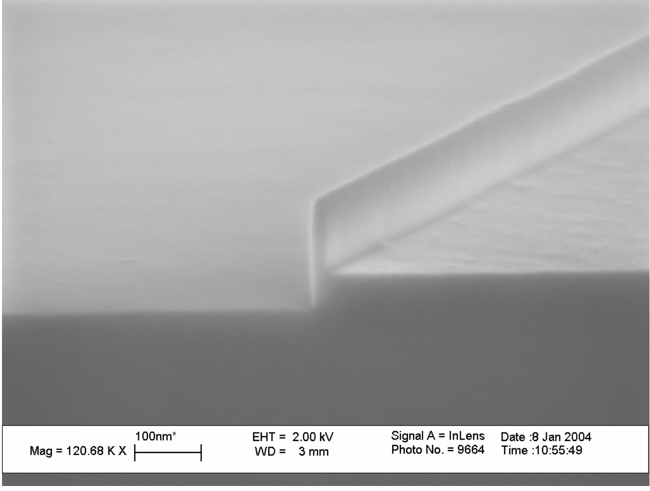


Figure 5-2: *20 nm wide nano-ridge with shorter second silicon etch step, causing a level difference.*

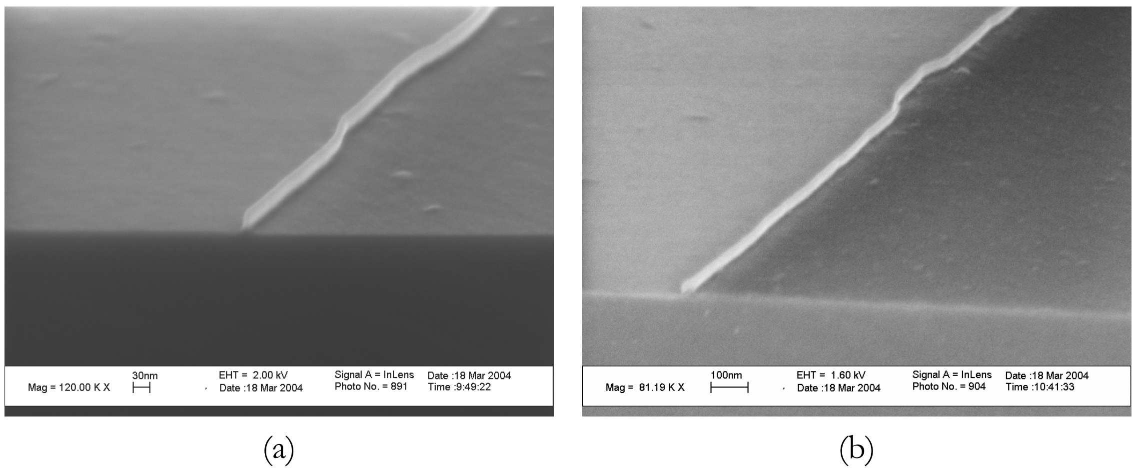


Figure 5-3: *(a) 15 nm wide nano-ridge with two identical silicon etch steps. (b) 7 nm wide nano-ridge with two identical silicon etch steps.*

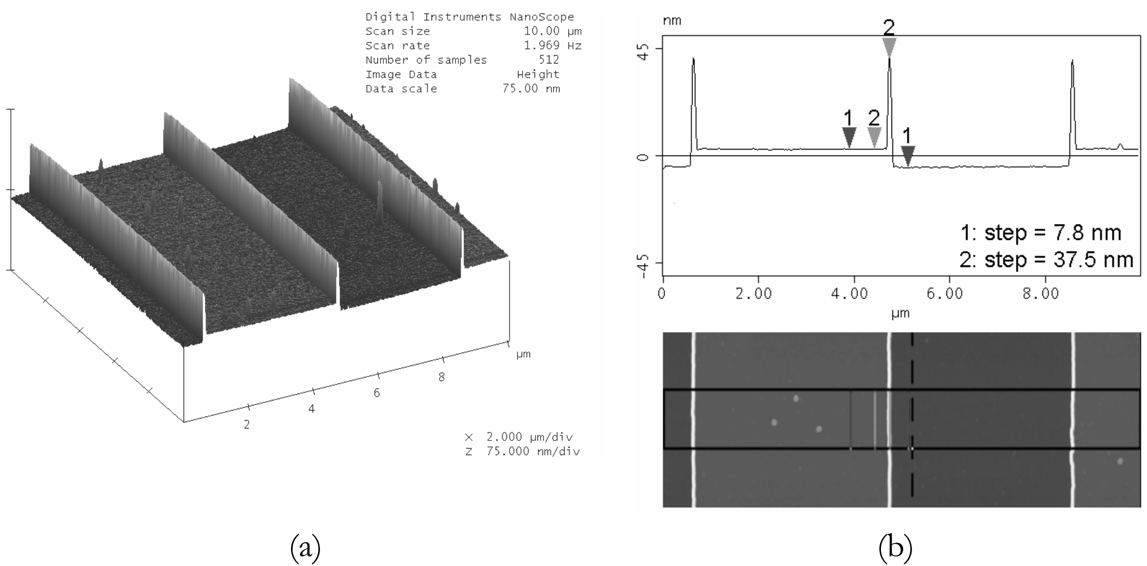


Figure 5-4: *AFM scans of 15 nm wide nano-ridges. (a) 3D view of the fabricated structures. (b) Section view with height measurements. The width of the edges cannot be accurately determined with AFM, due to the fact that an AFM picture is actually a convolution of the sample with the AFM tip, which has a limited radius (10 nm) and a finite aspect ratio (3:1).*

In all the cases, hardly any defects could be found on full wafer scale.

5.1.3 Etching selectivity of SiO_2/SiN_x in H_3PO_4

Based on the SEM pictures and on thickness measurements of the dry oxide layer before and after stripping of the nitride layer, the nano-ridges were observed to be a little less wide than the initial thickness of the grown dry oxide layer. This is due to the fact that not only the silicon was oxidized in the LOCOS step, but also the SiN_x mask was oxidized, if only a little bit [12, 14]. When stripping the SiN_x in step (f), this leads to a longer stripping time in H_3PO_4 than the time that was initially needed to etch the nitride mask in step (c) (because the H_3PO_4 has to break through the thin oxide covering the SiN_x layer before the bulk SiN_x can be etched). During this longer etch, also the dry oxide was exposed for a longer period to the phosphoric acid. This lead to a loss of 5 to 6 nm of the dry oxide in these experiments (as measured with a Plasmos SD 2002 ellipsometer). To try to improve the selectivity of SiN_x over SiO_2, a comparison between the etch rates of these materials in hot phosphoric acid was performed (this selectivity has been observed to improve when lowering the temperature of the H_3PO_4 [15]).

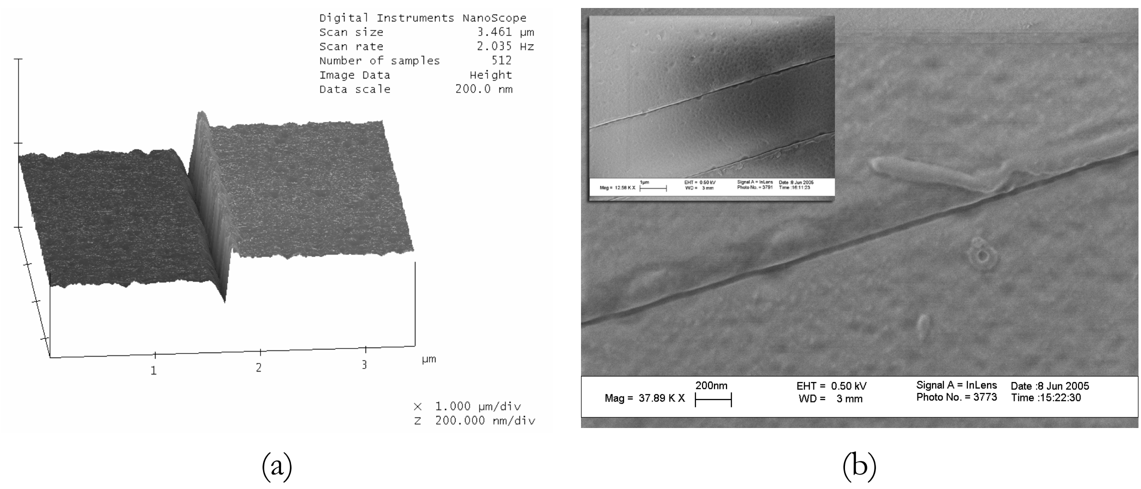
temperature [ºC]	**etch rate SiN_x [nm/min]**	**etch rate SiO_2 [nm/min]**	**Selectivity [-]**
180	4.1	0.48	8.5:1
160	1.4	0.16	8.9:1
140	0.5	0.05	8.6:1

Table 5-I: *Influence of temperature on etch rates of SiN_x and SiO_2 in hot phosphoric acid.*

The results of this experiment (Table 5-I) show that lowering the temperature had no significant effect on the selectivity in our case. However, the absolute silicon dioxide and silicon nitride etch rates dropped significantly (approximately a factor of 3 for each 20 degrees of temperature difference), but for our purpose this was not useful. An option would be to use a nitride that oxidizes slower at 950ºC, for example stoichiometric Si_3N_4 [12]. This could also have consequences for the selectivity of nitride/oxide. However, this option has not been explored, because the current selectivity (approximately 9:1) was enough to demonstrate the proof of principle of the technology.

5.1.4 Nano imprint lithography using nano-ridges as a stamp

Imprints of the nanostructures were made using hot embossing in PMMA (the glass temperature T_{glass} of PMMA 105ºC). Before imprinting, the stamps were coated with an anti sticking layer (a self assembled monolayer of fluoroalkyl). The imprinting temperature was 180ºC (two minutes heating up), the imprint pressure was 40 bar, and the cooling down time was around 20 minutes. The samples were separated at a temperature of approximately 108ºC (just above the glass temperature of the PMMA). Any residue of PMMA in the imprinted slits can be removed in an O_2 plasma etch step. Figure 5-5(a) shows an AFM scan of the PMMA layer after imprinting with the 20 nm wide, "2-level" nano-ridges from Figure 5-2.



(a) (b)

Figure 5-5: *Imprints of 20 nm wide nano-ridges in PMMA. (a) AFM image of the imprinted layer (notice the level difference. (b) SEM picture of the imprinted PMMA layer (insert: lower magnification view).*

It is difficult to say anything about the dimensions of the imprinted structure based on the AFM picture, due to AFM tip convolution effects. However, the level difference as measured by AFM was 51 nm, and this is in good agreement with our calculations (based on the unequal silicon etching steps) and with the SEM picture in Figure 5-2. Figure 5-5(b) shows a SEM image of the imprinted PMMA layer: detailed inspection of close-ups showed that the trench width is in fact in the order of 20 - 40 nm.

5.1.5 Possible extensions of this technology

In the present case, the combination of anisotropic wet etching and the crystal orientation of the <110> wafers limits us to straight trenches with vertical sidewalls in the <110> direction only. On a <110> wafer, only two orientations of the mask give channels with vertical sidewalls: parallel to the primary or the secondary flat of the wafer (see also Figure 1-3). When arbitrary shaped structures are desired, RIE (instead of wet anisotropic etching) could be used to transfer the pattern into the silicon substrate. RIE etching is able to produce arbitrary shaped structures with near-vertical sidewalls. Nevertheless, they are usually slightly tapered and not as smooth as the walls obtained by wet anisotropic OPD 4262 etching, leading to a less well defined geometry of the final structure. An example of such a technology can be found in [8].

5.1.6 Conclusions

We have successfully fabricated silicon oxide nano-ridges, based on standard optical photolithography and wet etching techniques. Wafer scale structures, with a variable width and height in the sub-50 nanometer range were produced. Line-widths ranging from 7 - 20 nm have been obtained, while the height can be varied from around 20 nm to a few hundred nanometers. The process delivers defect-free structures over a large area, and can be adapted using RIE to comprise various geometries, by modifying the photolithography mask design to suit specific needs.

5.2 2D nanochannel fabrication using laser interference lithography and wet anisotropic etching of silicon

An alternative technique to create two dimensional nanostructures is by laser interference lithography (LIL) [16-19]. LIL uses the interference pattern of two intersecting beams of laser light to expose a resist layer. Using this method, periodic structures (gratings and arrays of holes or dots) can be produced, with grating periods down to half of the laser wavelength.

A clear advantage of LIL over other resist patterning techniques, such as E-beam lithography, FIB, or AFM writing, is the fact that LIL can be used to expose large areas in one exposure: depending on the type of LIL set-up and resist choice complete wafers can be exposed in minutes, or even seconds. For applications such

as photonic crystals [20-24], information data storage [25, 26], or for instance fluidic filters [27, 28], LIL is an attractive alternative for the conventional lithography technologies.

In the following paragraph, the LIL set-up will be described briefly, after which resist choice will be discussed, followed by a combination of LIL generated patterns and anisotropic wet etching of silicon using OPD 4262 as the etchant to obtain true 2D nanochannel structures. Finally, reproduction of these structures using nano imprint lithography will be briefly discussed.
The process documentation used for the fabrication of the nanochannels can be found in the Appendix.

5.2.1 Set-up and principle of operation

The basic principle of laser interference lithography is shown in Figure 5-6:

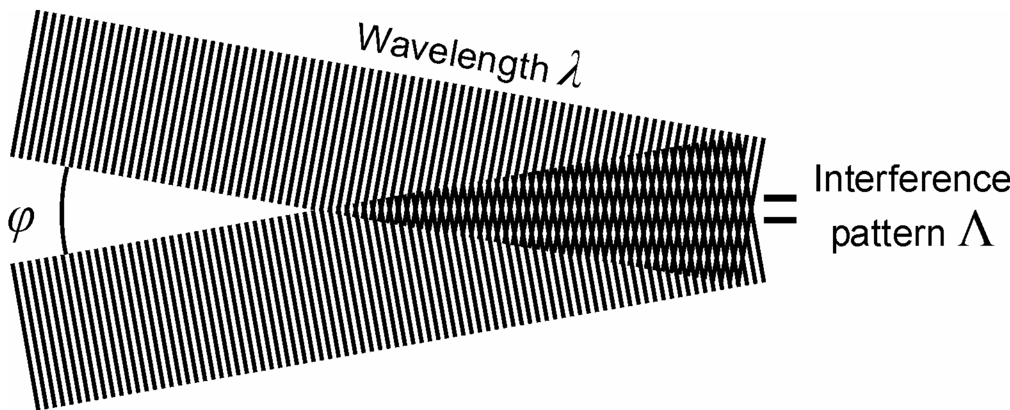


Figure 5-6: *Laser interference lithography principle of operation.*

The two intersecting, planar and coherent laser beams create an interference pattern with a period Λ. This period depends on the wavelength λ and the spatial angle φ between the two beams, as is shown in equation (5.1):

$$\Lambda = \frac{\lambda}{2\sin\left(\frac{\varphi}{2}\right)} \tag{5.1}$$

The theoretical limit for the period, which follows from this formula, is $\lambda/2$. The highest angle which can be used in practice is 140 degrees for our system. This is

due to edge effects of the mirror during the exposure at high angles in the Lloyd's mirror set-up, which is described below.

There are two major LIL set-up configurations: the Lloyd's mirror configuration [29] and the dual beam set-up. Both are depicted in Figure 5-7.

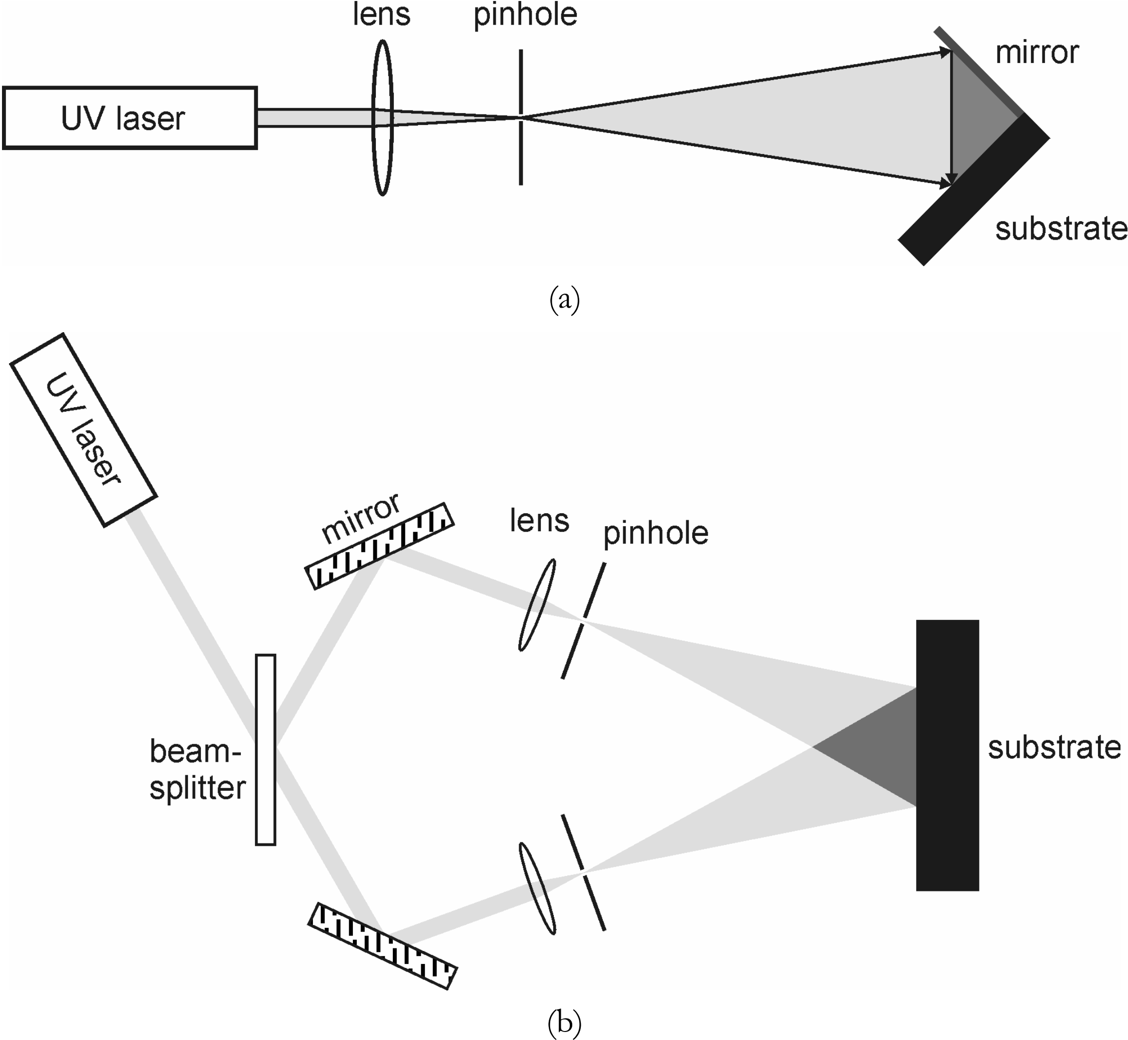


Figure 5-7: *Two possible LIL configurations. (a) Lloyd's mirror set-up. (b) Dual beam system.*

The Lloyd's mirror type set-up was used in the experiments described in this section. Because typical exposure times are several tens of seconds, the Lloyd's mirror set-up is easier to control, as external disturbances (mainly vibrations in the table) are not influencing the interference pattern. The dual beam set-up is more vulnerable to external disturbances, because the beam is split early in the optical

path, and any vibrations in for instance the mirrors during exposure will result in a shift of the position of the interference pattern at the place of the substrate. As the laser, a four times frequency doubled Nd:Yag laser is used, resulting in a wavelength of 266 nm.

5.2.2 Resist selection

For the combination of LIL with wet anisotropic etching of <110> silicon wafers, three different types of resists were examined:

- Diluted Olin 907-12: a diluted version of the standard positive photoresist used in the normal wet etching processes. It is diluted as follows: EEP:MMP:Olin 907/12 = 6:4:10 (EEP = ethyl-3-ethoxypropionate and MMP = methyl-3-methoxypropionate).
- Clariant AZ 1505 (a positive photoresist with a layer thickness of 500 nm when spun at 4000 rpm).
- MicroChemicals TI04XR image reversal resist (a custom version of the commercially available TI09XR resist).

The main criteria for resist selection are: layer thickness, adhesion to the substrate, and resist profile after development. The TI04XR resist can operate both in positive mode and in image reversal mode (an image reversal bake step is added to the process in this mode, followed by a flood exposure).

5.2.3 Pattern generation with LIL

A standard HNO_3 cleaning step was applied to all silicon wafers. Then a HMDS layer (liquid or vapor phase) was deposited on the wafers as an adhesion promoter for the resist. Following this, the photoresist was spun on the wafers. The process parameters which were used for the different types of resist can be found in Table 5-II.

After resist coating the wafers were exposed on the LIL system in Lloyd's mirror configuration, using a ($\varphi/2$) angle of 15.4 degrees. This resulted in a line pattern with a period of 500 nm (using a wavelength of 266 nm).

resist	spinning speed	spinning time	prebake @ 95°C	thickness	exposure time @ 150 μW/cm^2
Dil. Olin	3200 rpm	30 s	5 min	0.4 μm	35 s
TI04XR	4000 rpm	30 s	1 min	0.4 μm	50 s
AZ 1505	4000 rpm	30 s	1 min	0.5 μm	13 - 17 s

Table 5-II: *Resist spinning and LIL exposure parameters.*

After exposure the TI04XR resist could be directly developed (positive mode). Alternatively an image reversal bake (4 min @ 130°C), followed by a flood exposure under a mask aligner (12 s @ 9 mW/cm^2) could be applied to create a negative image in the photoresist layer (some properties of this photoresist, such as resistance to HF etching, only function well in image reversal mode due to the added polymer cross-linking during the image reversal procedure).

Following the exposure in the LIL system, the resist pattern was developed in standard OPD 4262 developer (60 s). Resist profiles were determined under a high resolution scanning electron microscope. Pictures can be found in Figure 5-8.

The following observations were made, based on the exposure and development results for the different types of resist:

Figure 5-8(a+b): The diluted Olin 907/12 photoresist showed good uniformity and profile under the SEM, and is a good candidate for use with laser interference lithography.

Figure 5-8(c+d): The Clariant AZ 1505 resist showed poor performance: the resist could not be developed to produce a resist pattern with a good profile. This resist was not used any further.

Figure 5-8(e+f): MicroChemicals TI04XR showed a good profile (also in positive mode).

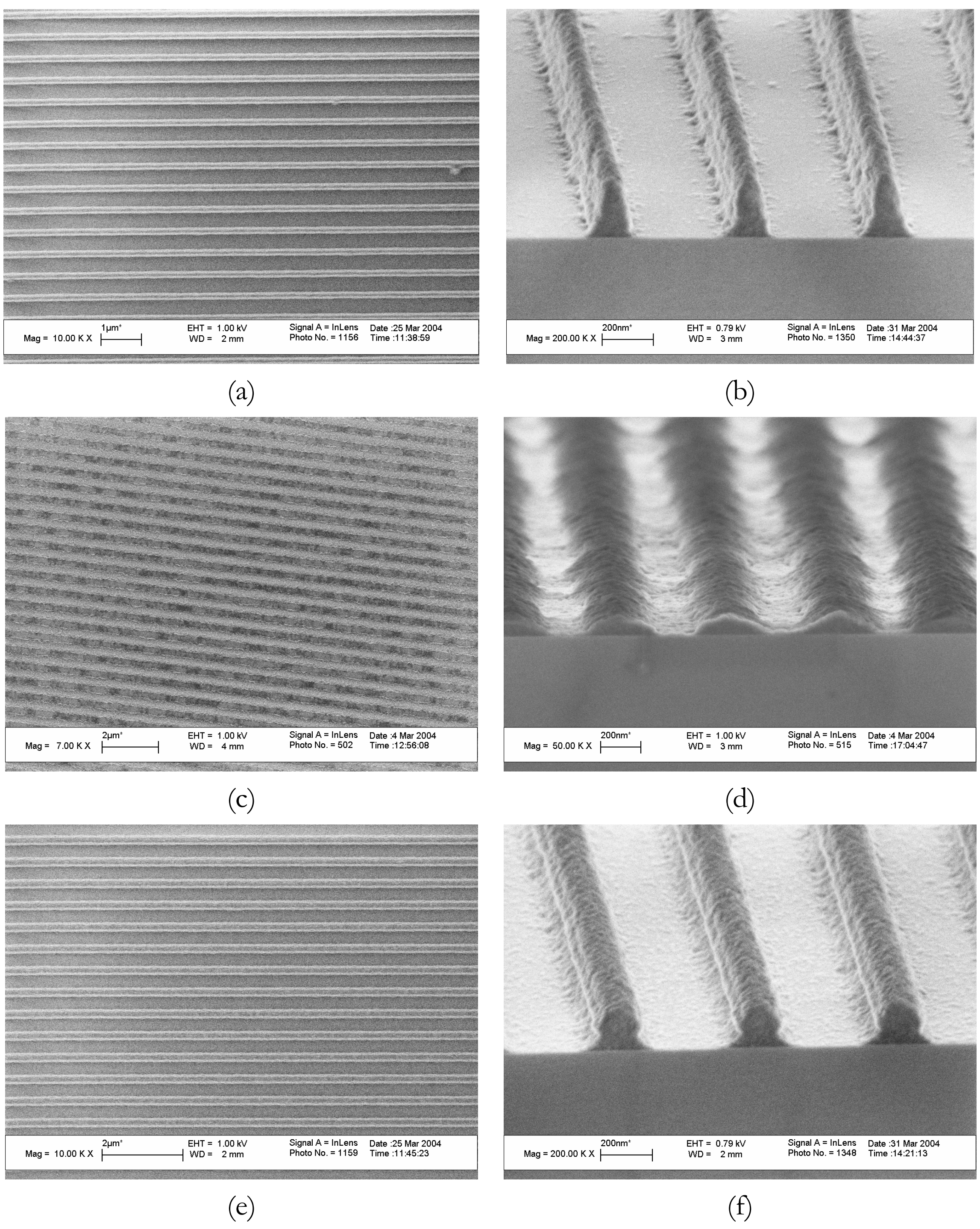


Figure 5-8: *SEM pictures of developed photoresist layers with LIL line patterns (500 nm period). (a+b) Diluted Olin 907/12 resist. (c+d) Clariant AZ 1505. (e+f) MicroChemicals TI04XR (in image reversal mode).*

The developed photoresist lines showed a ripple in the vertical walls of the resist. This is due to vertical standing waves in the photoresist during LIL exposure. A way to avoid these is the use of a bottom anti reflective coating (BARC) between

the silicon substrate and the photoresist layer. This layer was not included in the process because the BARC can not be wet-etched anisotropically; an extra RIE step would have been necessary, making the process less controllable (stopping the RIE exactly on the native oxide layer is not trivial).

5.2.4 Wet pattern transfer to silicon

After development, the wafers with the LIL line patterns (diluted Olin 907/12 and TI04XR resist) were etched following the standard OPD 4262 etching process. For clarity, this process is repeated in short:

1. 1% HF (or BHF) etching (transfer of the resist pattern to the native oxide).
2. H_2O dip to remove excess HF.
3. Resist stripping (1 min acetone, 1 min isopropanol, N_2 blow-dry).
4. OPD 4262 silicon etching.

The following observations were made:

HMDS priming and resist adhesion

Liquid phase HMDS priming of the wafers gave insufficient adhesion of the photoresist to the substrate, and thus delaminating of the resist during wet etching of the native oxide layer. Vapor phase HMDS priming showed sufficient adhesion.
TI04XR in positive mode can not stand the wet etching steps. Use of the positive mode is therefore not advised.
TI04XR (in image reversal mode) and diluted Olin resist showed good adhesion during the wet etching process.

Pattern transfer

The resulting channels have a smoother bottom surface when BHF is used to transfer the resist pattern to the native oxide layer (instead of 1% HF). This is probably caused by the higher oxide etch rate of BHF, thus more of the resist residue which was left after development (Figure 5-8(b+f)) was removed by underetching. However, the use of BHF makes the channel width less controllable, because of the underetching of the resist lines themselves. Also, as we have seen in the previous chapters, BHF etches silicon at room temperature. This, in

combination with the resist residue after development, could lead to a roughening of the channel bottom.

In general, the TI04XR photoresist gave the best results. A picture of 2D nanochannels created using TI04XR image reversal resist in combination with wet anisotropic etching of <110> silicon (using OPD 4262), can be found in Figure 5-9. The channel width and depth are approximately 300 nm and 140 nm, respectively.

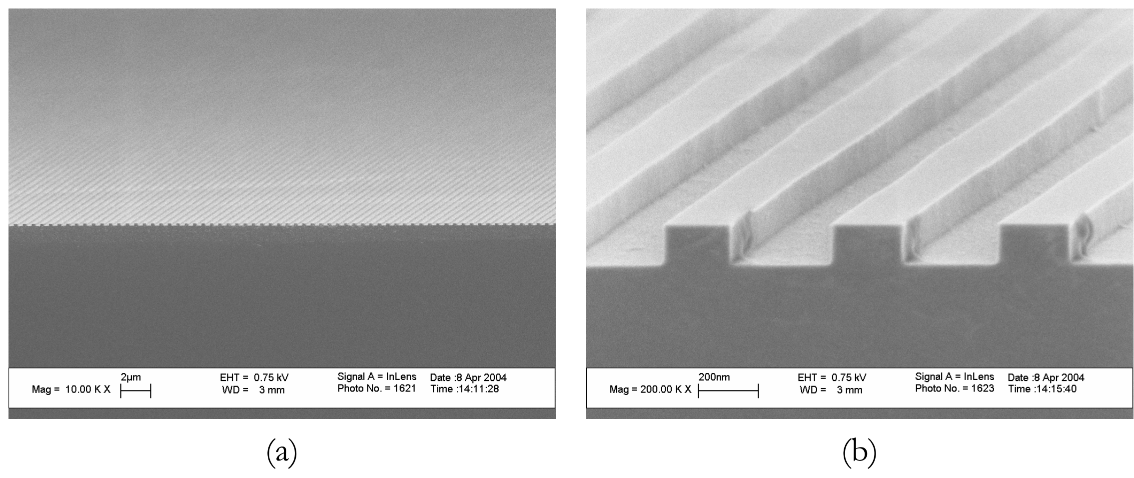


Figure 5-9: *Pictures of cross-sections of 2D nanochannels etched in <110> silicon with OPD 4262 (etching time = 30 minutes) and a 500 nm period LIL pattern. (a) Overview. (b) Close-up.*

5.2.5 Nano imprint lithography using LIL channels as a mould

Some introductory experiments were done to study the applicability of the fabricated 2D nanochannels as master molds for nano imprint lithography.

The silicon substrates with 2D nanochannels structures (the stamps) were cleaned in piranha solution (3:1 ratio of concentrated H_2SO_4 and 33% aqueous H_2O_2) for 15 minutes, together with bare silicon substrate wafers. An anti-adhesion layer (1*H*,1*H*,2*H*,2*H*-perfluorodecyl-trichlorosilane or -triethoxysilane) was applied to the stamps after cleaning in order to facilitate the de-molding process after imprinting. The bare silicon substrates were then covered with a 400 nm thick layer of Poly(methyl methacrylate) (PMMA: MW 350 kD, Aldrich: 40 g/L in toluene) by spin coating (20 s @ 2000 rpm). Stamp and substrate were placed parallel and brought into contact applying a pressure of 40 bars at a temperature of 180°C

(approximately 75 degrees above the glass temperature of PMMA) using a hydraulic press (Specac). After imprinting the system was cooled down (during 20 minutes). Demounting and separation of stamp and substrate took place just before the temperature reached the T_{glass}. The residual layer after imprinting could be removed by O_2 plasma during 20 s in a reactive ion etching system.

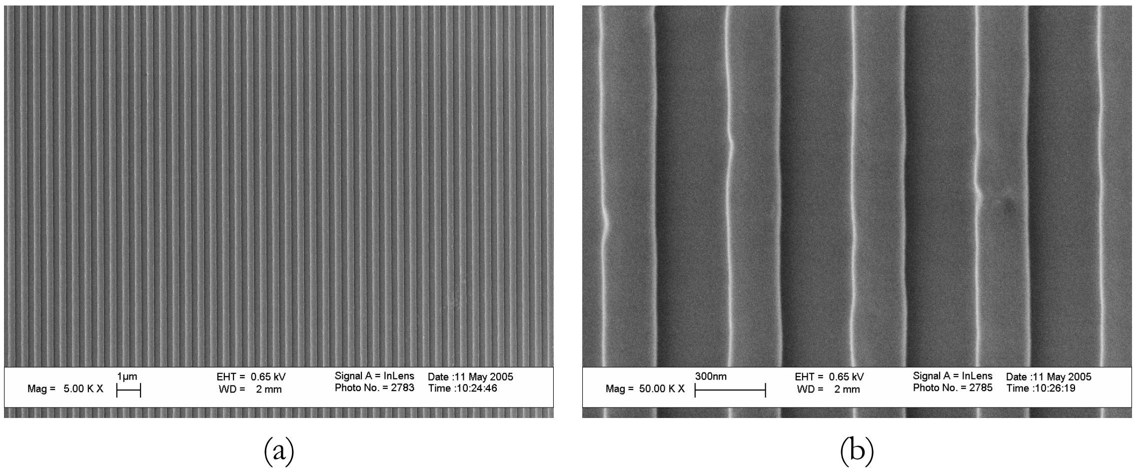


Figure 5-10: *Results of nano imprint lithography performed with 2D nanochannels from Figure 5-9.*

Large scale pattern transfer with little or no defects was achieved, as can be seen in Figure 5-10. Similar to the previously produced nano-ridges, nano imprint lithography is a good method for reproducing these nanostructures.

5.2.6 Conclusions

Two dimensional nanochannels were successfully fabricated using a line pattern generated by laser interference lithography, together with the previously described wet anisotropic etching process on silicon <110> wafers. It was observed that the use of a vapor phase HMDS priming system is essential for a good adhesion of the various photoresists to the silicon substrates. When using liquid phase (spin coating) HMDS, the resist delaminated during the pattern transfer process. OPD 4262 wet etching of silicon produced channels with smooth sidewalls and bottoms.
Of the three tested types of photoresist, MicroChemicals TI04XR (used in image reversal mode) gave the best results. The image reversal procedure could be further optimized for better resist performance and results.

5.3 Conclusions

Two methods for the production of two dimension nanochannels are presented in this chapter. Both have advantages over “normal” nanolithography technologies, such as E-beam lithography, focused ion beam lithography or AFM writing techniques. The advantages mainly consist of the possibility to create patterns on wafer-scale (although the LIL set-up is limited to an exposure area of several square centimeters in Lloyd’s mirror configuration: the dual beam set-up can expose full 100 mm wafers or even larger). The advantage of the nano-ridge fabrication method over LIL is that it can be relatively easily modified to create 2D nanostructures of arbitrary shape, by using RIE etching instead of OPD 4262 wet etching of <110> silicon. On the other hand, LIL can generate patterns of lines (or holes, for that matter) in a matter of seconds, but it is limited to channel widths down to approximately 100 nm. The SiO_2 nano-ridge technology, in combination with nano imprint lithography, can be used to create even smaller channels, but is limited in ridge-to-ridge distance (or channel density). This is because of the use of common optical lithography to define the location of the nano-ridges.

A logical next technological step is to combine the two technologies, in which case the special frequency doubling effect of the nano-ridge fabrication method can be used to reduce the period of the LIL structures to half of its original value, while still creating sub-25 nm wide structures.
Finally, wafers with 2D level nanotopography should be bonded with a second processed wafer to enable fluidic experiments.

5.4 Acknowledgements

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6

Conclusions and outlook

In this chapter the main conclusions of the previous chapters are recapitulated. In addition, some ideas about the future of nanofluidic channel fabrication and characterization will be given.

6.1 Summary of conclusions

In this thesis, many aspects involved in the fabrication and characterization of nanochannels have been treated.

The results from chapter two and three are very valuable for those people wishing to create 1D nanochannels in silicon. In the depth range of 50-500 nm, the use of wet anisotropic etching of <110> silicon wafers yields very well-defined channels with smooth and vertical sidewalls, combined with very low channel bottom roughness. As the etchant Olin OPD 4262 developer can be used (having a Si <110> etch rate of 3.7 nm/min at room temperature).
Uniformity across a wafer was measured to be within ± 2% of the etch depth, for a wafer full of 4 μm wide and 50 nm deep channels. However, when etching nanochannels using the chip design from chapter three, the channel depth variation was observed to be increased (± 10% of the mean channel depth). Ultrasonic agitation of the etchant during etching improved the uniformity notably to ± 5%.
The surface roughness on the bottom of the etched channels was measured to be approximately 0.3 nm RMS. The native oxide already present on the wafers is sufficient to be used as a mask material during the wet etching process. If channel depths larger than 500 nm are desired, the use of a pre-grown mask (such as a very thin layer of silicon dioxide) is required. The very low underetch rate makes this technique also suitable for nanochannels with a very small width.

When very small channel depths are desired, the limitations of the wet anisotropic etching technique (etch speed, start-up effect), make a more accurate technology necessary. In this regime, a spacer layer of dry oxide can be used to define the height of the channels. Channels with depth down to 5 nm have been fabricated by selectively etching of the dry oxide layer with hydrofluoric acid.
Advantages of this method are the good control over the thickness of the layer (using dry oxidation at a temperature of 950ºC), and the very low surface roughness of the channels (RMS value below 0.2 nm). Furthermore, the thickness of the layer (and thus the resulting channel height) can be measured by ellipsometry, making the use of mechanical profilometry (which is less accurate at these dimensions)

obsolete. The uniformity of the oxide layers was measured to be very good: variations over the used wafer area were less than ± 3%.
Care must be taken in selecting the wet chemical etchant for the dry oxide layer: it was observed that buffered HF etchant etches not only the silicon dioxide layer, but also the underlying silicon, leading to a larger than expected (and desired) channel depth. The use of dilute (1%) hydrofluoric acid does not create this problem (but precautions must be taken to prevent photoresist delaminating).
The downside of this channel fabrication method is that the resulting channels do not have a rectangular cross-section, due to the isotropic wet etching of the spacer layer (applications involving 2D nanochannels with a rectangular cross-section are not feasible using this method).

Furthermore, in chapter three nanochannel chips were fabricated from <110> silicon wafers. The chip design includes 1D fluidic nanochannels, measurements rulers and fluidic reservoirs. The channels were sealed by bonding the silicon wafers to Borofloat cover wafers containing powder blasted fluidic access holes. Chips with approximate depths of 50, 100 and 150 nm have been fabricated using the wet anisotropic etching technology from chapter two. Smaller channel depths (ranging from 50 nm down to 5 nm) were realized using the dry oxide spacer layer technology, from the same chapter. Once again it was confirmed that for best results, 1% HF should be used as the etchant for the oxide etching step.

A model for the capillary filling of the fabricated nanochannels was presented in chapter four. The Washburn equation, modified for the rectangular cross-section of the channels, was used to describe the position of the liquid meniscus in the channel during the filling process. Filling of the chips (fabricated using wet anisotropic etching of silicon) with DI water and 0.1 M NaCl (aq) showed that the filling qualitatively follows the Washburn model very well. Quantitatively, there were some deviations from the model. The deviations became larger with decreasing channel height. For DI water in the 50 nm deep channels, the apparent viscosity was 24 ± 11% higher than the bulk viscosity of water. The increase in apparent viscosity was attributed to the electroviscous effect. This is supported by the fact that the effect is much less pronounced when using the 0.1 M NaCl solution instead of DI water. The much smaller electric double layer thickness and

much higher conductivity in the salt solution largely reduces the electroviscous effect.

Filling of the smallest channels, fabricated using the dry oxide spacer technology in combination with 1% HF etching, was performed using cyclohexane and water. A deviation from the model was also observed here, expressed as a correction factor C, which was as large as 1.6 ± 0.4 for filling with cyclohexane and 2.6 ± 0.4 for filling with water (in the 5 nm deep channels). This can not be satisfactorily explained by an electroviscous effect; other possible explanations include a very thin, highly viscous layer of quasi-stationary molecules next to the channel wall, or elastic deformation of the channels due to the high negative pressures associated with capillary filling. Another (small) deviation from the expected Washburn behavior is observed in the smallest channels. This deviation can be described by a constant loss of liquid per unit time at the meniscus (6 μm/s for cyclohexane and 8 μm/s for filling with water), due to for instance corner flow or evaporation of liquid at the meniscus.

In chapter five two possible methods for the fabrication of two-dimensional nanochannels (having a width which is also in the nanometer range) were discussed and explored. It is possible to fabricate large, defect free arrays of nano-ridges by using a LOCOS process in combination with wet anisotropic etching of <110> silicon. Arrays of SiO_2 nano-ridges, having widths between 7 and 20 nm and heights of 20 nm and more, have been fabricated.

A different technique is the use of laser interference lithography to create large amounts of parallel lines in photoresist. Several different types of resist were examined and optimized. Subsequent wet etching using OPD 4262 produced channels with a width of 300 nm and a height around 140 nm in <110> silicon. These dimensions can be varied by changing the interference angle and/or the wet etching time.

Reproduction of all 2D nanostructures was demonstrated using nano imprint lithography. This produced 1:1 negative replicas of the structures in PMMA.

6.2 Outlook

The production of nanochannels, whether one- or two-dimensional, is gaining more and more attention. Still, not a lot is known about the behavior of liquids in nano-confinement. With the technology presented here, it is possible to do experiments with various liquids (other than the already mentioned ones), and thus gain more understanding about fluid flow in nanochannels. Interesting experiments would for instance be charge exclusion experiments (based on massive double layer overlap in ultra shallow nanochannels), or chromatography in nanochannels. Also, fluid flow in 2D nanochannels can be studied.

The effect of the thickness of the oxide on the channel bottom on the apparent viscosity of liquids during capillary filling is also a subject which should be explored. By varying the thickness of the insulating oxide layer, manipulation of the electroviscous effect could be possible (due to the fact that generation of the streaming potential is suppressed by the conductivity of the silicon base). Expanding on this subject, electro-osmotic flow can be performed in these nanochannels by integrating electrodes in the design.

Other useful research would be to try to model the channel deformation under large negative pressure. This is of vital importance if one wishes to compare the experimental results quantitatively to the Washburn model.

Furthermore, during filling of the channels bubbles are sometimes formed by enclosure of air at the moving liquid front. The bubble generation process is not well understood: by introducing defects, such as bumps or dents in the channel or in the channel wall, more knowledge about this interesting phenomenon can be gathered.

When looking at the fabrication technology, it is of interest to use other sealing technologies for the nanochannels, for instance by replacing the Borofloat cover wafer by a thin layer of silicon nitride and studying mechanical deformation of the membrane during capillary filling.

The BHF overetch effect could also have some very interesting benefits. If this can be applied in a controlled way, fabrication of even smaller channels is possible. A sequence of wet chemical oxidation, stripping in 1% HF, wet chemical oxidation, stripping etc., is likely to produce more reproducible results, though. Based on the current experiments, channels with a depth of 0.7 nm should be possible to fabricate. In this case, care has to be paid that the width of the channel should also be reduced, as the Vanderwaals forces or bending of the wafers can cause the channel to collapse if the channel depth becomes too low.

Appendix: Process documentation

In this appendix, the fabrication processes for the creation of nanochannel chips using wet anisotropic etching of <110> silicon, or by a dry oxide spacer layer are described in detail. Furthermore, the process recipe for the fabrication of silicon dioxide nano-ridges is given, as well as the 2D nanochannel fabrication process using laser interference lithography and wet anisotropic etching of <110> silicon.

A.1 Nanochannel chip fabrication process

A.1.1 Mask layout and process outline

Mask layout

Three masks are necessary:
PB: powder blasted holes.
CHAN: nanochannel definition.
RIE: reactive ion etching of reservoirs and rulers.

Process outline top (Borofloat) wafer

Nr	Process steps	Cross-section after process
I - IV	Double sided lithography: bonding side 50 μm non-bonding side 100 μm Mask: **PB**	
V - VI	Powder blasting through wafer	

Process outline bottom (<110> silicon) wafer

OPD 4262 SILICON ETCHING PROCESS			DRY OXIDE SPACER LAYER PROCESS		
Nr	**Process steps**	**Cross-section**	**Nr**	**Process steps**	**Cross-section**
1	<110> Si wafer with native SiO_2		1 - 5	<110> Si wafer with dry SiO_2 spacer	
2 - 6	Lithography mask: **CHAN**		6 - 11	Lithogaphy mask: **CHAN**	
7a	1% HF native oxide etch		12 - 13	1% HF channel etch + resist strip	
7b	OPD 4262 channel etch + mask strip		14 - 19	Lithography mask: **RIE**	
8 - 13	Lithography mask: **RIE**		20 - 21	RIE etching of reservoirs	
14	RIE etching of reservoirs		22 - 24	Resist strip/ cleaning	
15 - 18	Resist strip/ dry oxidation				

Process outline wafer bonding

OPD 4262 silicon etching process			Dry oxide spacer layer process		
Nr	**Process steps**	**Cross-section**	**Nr**	**Process steps**	**Cross-section**
A - E	Cleaning + bonding + annealing		A - E	Cleaning + Bonding + annealing	

A.1.2 Top wafer processing (Borofloat)

Nr	Process	Parameters	Remarks
I	**Lithography - Lamination of BF405 foil** (#lith033)	ELTN7143/4 / GBC 3500Pro Laminator Ordyl BF405 dry resist foil • Temp: 130°C ('Carry' preset) • Speed: 2 ('Carry' preset)	Protection of direct bonding side against scratching.
II	**Lithography - Lamination of BF410 foil** (#lith032)	ELTN 7143/4 / GBC 3500Pro Laminator Ordyl BF410 dry resist foil • Temp: 130°C ('Carry' preset) • Speed: 2 ('Carry' preset)	
III	**Lithography - Alignment & Exposure BF410 foil** (#lith034)	ELTN7143/4 / Exposure Tool • Time: 30sec	Mask: **PB**.
IV	**Lithography - Development BF410 foil** (#lith036)	ELTN7143/4 / HCM Spray Developer Na_2CO_3: MERCK 1.06392.0500 Na_2CO_3:H_2O = 15g : 7.5liters (+ 1 cup Antifoam) • Temp: 32°C • Time: 3min • Rinsing • Spin drying	Due to non-uniform development turn sample by 180° after 90 s. Small features might need longer development time.
V	**Powderblasting of Glass - low resolution** (#etch020)	ELTN10156 / Powder blaster For feature size >100μm • Particles: 30μm AlO_2 • Pressure: 4.6bar • Mass flow: 3-12 g/min • Etchrate appr. 91μm per g/cm^2	Etch through wafer (1 mm). File actual parameters in logbook.
VI	**Resist stripping**	- rinse in DI - spin drying - transport wafer to clean room - strip foil in acetone (user made) - rinse in DI - final ultrasonic clean in DI, 10 min - spin drying	

A.1.3a Bottom wafer processing (OPD 4262 silicon etching process)

Nr	Process	Parameters	Remarks
1.	**Substrate selection Silicon <110> DSP** (#subs010)	CR112B / Wafer Storage Cupboard Orientation: <110> Diameter: 100mm ± mm Thickness: 380µm ± 10 µm Polished: Double side polished (DSP) Resistivity: 5-10Ωcm Type: p	Select <110> wafers.
2.	**Cleaning Standard** (#clean003)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
3.	**Lithography - Priming (liquid)** (#lith001)	CR112B/Suss MicroTech Spinner (Delta20) Hotplate 120°C HexaMethylDiSilazane (HMDS) • Dehydration bake (120°C): 5min • Spinning acceleration: 4000rpm/s • Spinning speed: 4000rpm • Spinning time: 20s	
4.	**Lithography - Coating Olin907-12** (#lith004)	CR112B/Suss MicroTech Spinner (Delta20) Hotplate 95°C Olin 907-12 • Spinning acceleration: 4000rpm/s • Spinning speed: 4000rpm • Spinning time: 20s • Prebake (95°C): 60s	
5.	**Lithography - Alignment & Exposure Olin 907-12 (EV)** (#lith020)	CR117B / EVG 20 Electronic Vision Group 20 Mask Aligner • Hg lamp: 12 mW/cm ^{2} • Exposure Time: 3.5 sec	Mask: **CHAN**.
6.	**Lithography - Development Olin Resist** (#lith011)	CR112B / Wet-Bench 11 Developer: OPD 4262 Hotplate 120°C (CR112B or CR117B) • After Exposure Bake (120°C): 60sec Development: • Time: 30sec in Beaker 1 • Time: 15-30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	

Nr	Process	Parameters	Remarks
7.	**Etching of Silicon by TMAH - ultra slow etch** (#etch049)	CR116B / Wet-Bench 2 Olin OPD 4262 A HF (1%) dip must have preceded this etching step • Temp.: 25°C • Quick Dump Rinse <0.1µS • Spin drying Etchrate (Si <110>) = 3.7nm/min	1% HF SiO_2 etch 1min Acetone 1min IPA OPD 4262 Si etch 1min HF mask strip QDR rinse Spin dry
8.	**Cleaning Standard** (#clean003)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
9.	**Lithography - Priming (liquid)** (#lith001)	CR112B/Suss MicroTech Spinner (Delta20) Hotplate 120°C HexaMethylDiSilazane (HMDS) • Dehydration bake (120°C): 5min • Spinning acceleration: 4000rpm/s • Spinning speed: 4000rpm • Spinning time: 20s	
10.	**Lithography - Coating Olin907-12** (#lith004)	CR112B/Suss MicroTech Spinner (Delta20) Hotplate 95°C Olin 907-12 • Spinning acceleration: 4000rpm/s • Spinning speed: 4000rpm • Spinning time: 20s • Prebake (95°C): 60s	
11.	**Lithography - Alignment & Exposure Olin 907-12 (EV)** (#lith020)	CR117B / EVG 20 Electronic Vision Group 20 Mask Aligner • Hg lamp: 12 mW/cm^2 • Exposure Time: 3.5 sec	Mask: **RIE**.
12.	**Lithography - Development Olin Resist** (#lith011)	CR112B / Wet-Bench 11 Developer: OPD 4262 Hotplate 120°C (CR112B or CR117B) • After Exposure Bake (120°C): 60sec Development: • Time: 30sec in Beaker 1 • Time: 15-30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	

Nr	Process	Parameters	Remarks
13.	**Lithography - Postbake before Cryogenic DRIE** (#lith010)	CR112B Hotplate 120° • Time: 30min Heraeus Convection Furnace • Temp.: 150° • Time: >15min	Postbake for Cryogenic DRIE to avoid cracking of resist.
14.	**Plasma etching of Silicon - standard (Oxford)** (#etch013)	CR102A / Oxford Plasmalab 100ICP Structure width 20-200µm, depth up to 150µm Load: 10-50% Maskmaterials: Cr: 20nm or Olin907/12: 1.2µm or WOX or DOX: 1.0-1.5µm • Temp.: -110°C • SF_6 flow: 120sccm • O_2 flow: 0sccm • CM pressure: 10mTorr • ICP power: 600W • He pressure: 20mbar Cleaning step: • RIE power: 7.5W • V_{DC}: -40-55V • Time: 1min Silicon etching: • RIE power: 2.0W • V_{DC}: -15V • Time: 4 min Directional profile	Fluid delivery microchannel etching 20 micron deep.
15.	**Stripping of Olin PR - standard** (#lith016)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 20min • Quick Dump Rinse <0.1µS • Spin drying • Visual microscopic inspection	
16.	**Cleaning Standard** (#clean003)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
17.	**Etching HF (1%) Native Oxide** (#etch027)	CR112B / Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: >1min • Quick Dump Rinse <0.1µS • Spin drying	HF dip directly prior to oxidation.

<table>
<tr><th>Nr</th><th>Process</th><th>Parameters</th><th>Remarks</th></tr>
<tr><td>18.</td><td>Dry Oxidation (DOX) at 950°C of Silicon
(#depo031)</td><td>CR112B / Furnace A2
Standby temp.: 700°C
• Program: Dry-950
• Temp.: 950°C
• Gas: O_2
Growthrate:
<table>
<tr><th>Oxidation (min)</th><th>Si <100> oxide (nm)</th><th>Si <110> oxide (nm)</th></tr>
<tr><td>0</td><td>2.27</td><td>2.38</td></tr>
<tr><td>6</td><td>8.29</td><td>12.33</td></tr>
<tr><td>12</td><td>12.2</td><td>17.51</td></tr>
<tr><td>24</td><td>17.78</td><td>25.67</td></tr>
<tr><td>48</td><td>28.06</td><td>38.58</td></tr>
<tr><td>96</td><td>45.68</td><td>59.1</td></tr>
<tr><td>192</td><td>75.88</td><td>91.43</td></tr>
</table></td><td>Dry oxide growing (20 nm → 15 min).</td></tr>
</table>

A.1.3b Bottom wafer processing (dry oxide spacer layer process)

Nr	Process	Parameters	Remarks
1.	**Substrate selection Silicon <110> DSP** (#subs010)	CR112B / Wafer Storage Cupboard Orientation: <110> Diameter: 100mm ± mm Thickness: 380µm ± 10 µm Polished: Double side polished (DSP) Resistivity: 5-10Ωcm Type: p	Select <110> wafers.
2.	**Cleaning Standard** (#clean003)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
3.	**Etching HF (1%) Native Oxide** (#etch027)	CR112B / Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: >1min • Quick Dump Rinse <0.1µS • Spin drying	HF dip directly prior to oxidation.

<table>
<tr><th>Nr</th><th>Process</th><th>Parameters</th><th>Remarks</th></tr>
<tr><td>4.</td><td>Dry Oxidation (DOX) at 950°C of Silicon
(#depo031)</td><td>CR112B / Furnace A2
Standby temp.: 700°C
• Program: Dry-950
• Temp.: 950°C
• Gas: O_2
Growthrate:
<table><tr><th>Oxidation (min)</th><th>Si <100> oxide (nm)</th><th>Si <110> oxide (nm)</th></tr><tr><td>0</td><td>2.27</td><td>2.38</td></tr><tr><td>6</td><td>8.29</td><td>12.33</td></tr><tr><td>12</td><td>12.2</td><td>17.51</td></tr><tr><td>24</td><td>17.78</td><td>25.67</td></tr><tr><td>48</td><td>28.06</td><td>38.58</td></tr><tr><td>96</td><td>45.68</td><td>59.1</td></tr><tr><td>192</td><td>75.88</td><td>91.43</td></tr></table></td><td>Dry oxide spacer layer:

06 nm: 1 min 15 s
12 nm: 5 min 30 s
25 nm: 22 min 30 s
50 nm: 75 min 00 s</td></tr>
<tr><td>5.</td><td>Ellipsometer Measurement
(#char007)</td><td>CR118B / Plasmos Ellipsometer

Measure oxide thickness profile
(raster 15x15 measurement points)

Line scans: y=18.8mm
y=-1.65mm
y=-22mm
x=-35..35mm
# of points (x,y)=(36,3)</td><td>Dry oxide thickness.

Wafer map.

Oxide thickness at position of chips.</td></tr>
<tr><td>6.</td><td>Cleaning Standard
(#clean003)</td><td>CR112B / Wet-Bench 3-2
HNO_3 (100%) Selectipur: MERCK 100453
HNO_3 (69%) VLSI: MERCK 116445
• Beaker 1: fumic HNO_3 (100%), 5min
• Beaker 2: fumic HNO_3 (100%), 5min
• Quick Dump Rinse <0.1µS
• Beaker 3: boiling (95°C) HNO_3 (69%), 10min
• Quick Dump Rinse <0.1µS
• Spin drying</td><td></td></tr>
<tr><td>7.</td><td>Lithography - Priming (gas phase)</td><td>CR112B/HMDS Gas Phase Primer
• Set oven to 150˚C
• Wafers in
• Vacuum (1 bar - 26 inches Hg ≈ 0.1bar)
• N_2 flush (decrease to 1 bar - 10 inches Hg)
• Repeat the 2 former steps 3 times
• Vacuum (1 bar - 26 inches Hg = 0.1bar)
• Dehydration bake 30 min
• V-HMDS 5 minutes
• N_2 flush
• Vacuum (1 bar - 26 inches Hg ≈ 0.1bar)
• Repeat the 2 former steps 3 times
• N_2 flush</td><td></td></tr>
</table>

Nr	Process	Parameters	Remarks
8.	**Lithography - Coating Olin907-12** (#lith004)	CR112B/Suss MicroTech Spinner (Delta20) Hotplate 95°C Olin 907-12 • Spinning acceleration: 4000rpm/s • Spinning speed: 4000rpm • Spinning time: 20s • Prebake (95°C): 60s	
9.	**Lithography - Alignment & Exposure Olin 907-12 (EV)** (#lith020)	CR117B / EVG 20 Electronic Vision Group 20 Mask Aligner • Hg lamp: 12 mW/cm ^{2} • Exposure Time: 3.5 sec	Mask: **CHAN**.
10.	**Lithography - Development Olin Resist** (#lith011)	CR112B / Wet-Bench 11 Developer: OPD 4262 Hotplate 120°C (CR112B or CR117B) • After Exposure Bake (120°C): 60sec Development: • Time: 30sec in Beaker 1 • Time: 15-30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	
11.	**Lithography - Postbake standard** (#lith009)	CR112B / Hotplate 120°C • Time: 30min	
12.	**Etching HF (1%) user made** (#etch028)	CR116B / Wet-Bench 2 HF (1%) VLSI: MERCK 112629.500 • Quick Dump Rinse <0.1µS • Spin drying	1% HF etching of nanochannels (appr. 3 nm/min).
13.	**Stripping of Olin PR - standard** (#lith016)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 20min • Quick Dump Rinse <0.1µS • Spin drying • Visual microscopic inspection	
14.	**Cleaning Standard** (#clean003)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	

Nr	Process	Parameters	Remarks
15.	**Lithography - Priming (gas phase)**	CR112B/HMDS Gas Phase Primer • Set oven to 150°C • Wafers in • Vacuum (1 bar - 26 inches Hg ≈ 0.1bar) • N_2 flush (decrease to 1 bar - 10 inches Hg) • Repeat the 2 former steps 3 times • Vacuum (1 bar - 26 inches Hg = 0.1bar) • Dehydration bake 30 min • V-HMDS 5 minutes • N_2 flush • Vacuum (1 bar - 26 inches Hg ≈ 0.1bar) • Repeat the 2 former steps 3 times • N_2 flush	
16.	**Lithography - Coating Olin907-12** (#lith004)	CR112B/Suss MicroTech Spinner (Delta20) Hotplate 95°C Olin 907-12 • Spinning acceleration: 4000rpm/s • Spinning speed: 4000rpm • Spinning time: 20s • Prebake (95°C): 60s	
17.	**Lithography - Alignment & Exposure Olin 907-12 (EV)** (#lith020)	CR117B / EVG 20 Electronic Vision Group 20 Mask Aligner • Hg lamp: 12 mW/cm^2 • Exposure Time: 3.5 sec	Mask: **RIE**.
18.	**Lithography - Development Olin Resist** (#lith011)	CR112B / Wet-Bench 11 Developer: OPD 4262 Hotplate 120°C (CR112B or CR117B) • After Exposure Bake (120°C): 60sec Development: • Time: 30sec in Beaker 1 • Time: 15-30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	
19.	**Lithography - Postbake before Cryogenic DRIE** (#lith010)	CR112B Hotplate 120° • Time: 30min Heraeus Convection Furnace • Temp.: 150° • Time: >15min	Postbake for Cryogenic DRIE to avoid cracking of resist.
20.	**Etching BHF (1:7) user made** (#etch025)	CR116B / Wet-Bench 2 NH_4F/HF (1:7) VLSI: MERCK 101171.2500 • Quick Dump Rinse <0.1µS • Spin drying Etchrate thermal SiO_2 = 60-80nm/min Etchrate PECVD SiO_2 = 125/nm/min Etchrate TEOS SiO_2 = 180/nm/min Etchrate Pyrex #7740 = 20nm/min	Remove dry oxide on bottom of reservoirs prior to RIE. (t = 1 min 30 sec)

Nr	Process	Parameters	Remarks
21.	**Plasma etching of Silicon - standard (Oxford)** (#etch013)	CR102A / Oxford Plasmalab 100ICP Structure width 20-200µm, depth up to 150µm Load: 10-50% Maskmaterials: Cr: 20nm or Olin907/12: 1.2µm or WOX or DOX: 1.0-1.5µm • Temp.: -110°C • SF_6 flow: 120sccm • O_2 flow: 0sccm • CM pressure: 10mTorr • ICP power: 600W • He pressure: 20mbar Cleaning step: • RIE power: 7.5W • V_{DC}: -40-55V • Time: 1min Silicon etching: • RIE power: 2.0W • V_{DC}: -15V • Time: 4 min Directional profile	Fluid delivery microchannel etching: 20 micron deep.
22.	**Stripping of Olin PR - standard** (#lith016)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 20min • Quick Dump Rinse <0.1µS • Spin drying • Visual microscopic inspection	
23.	**Cleaning Standard** (#clean003)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
24.	**Ellipsometer Measurement** (#char007)	CR118B / Plasmos Ellipsometer Measure oxide thickness at centre of wafer Specific ellipsometer measurement points: (-2,38), (2,38), (-2,-38), (2,38) mm	 Consistent w. step5? Measure native oxide thickness.

A.1.4 Direct bonding procedure

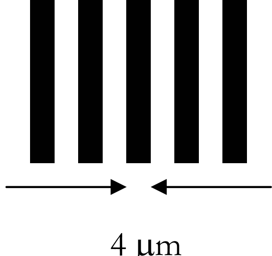
Nr	Process	Parameters	Remarks
Aa	**Cleaning Standard** (#clean003)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	Standard cleaning silicon wafers.
Ab	**Cleaning Glass** (#clean005)	CR112B / Wet-Bench 3-4 HNO_3 (100%) Selectipur: MERCK 100453 Use dedicated wafer carriers + glass rod! • Beaker 1: HNO_3 (100%) 5min • Beaker 2: HNO_3 (100%) 5min • Quick Dump Rinse <0.1µS • Spin drying	Standard cleaning Borofloat wafers.
B	**Cleaning "Piranha" (H_2SO_4/H_2O_2)** (#clean008)	CR112B / Wet-Bench 3-1 H_2SO_4 (96%) VLSI: MERCK 100709.2500 H_2O_2 (31%) VLSI: MERCK 108552.2500 Use dedicated wafer carriers and glass rod! H_2SO_4:H_2O_2 (3:1) vol% • add H_2O_2 to H_2SO_4 • exothermic process! • temperature 130°C • cleaning time 10-15min • Quick Dump Rinse <0.1µS • Spin drying	Silicon + Glass wafers. Store wafers in DI. Spin dry just before bonding: 1,5 min max speed.
C	**KOH dip** (for Borofloat wafers only)	CR102B / KOH KOH: MERCK 105019.500 KOH:DI = (1:3) 25wt% KOH: 500g KOH pellets in 1500ml DI water • Temp.: 75°C • Stirrer • Quick Dump Rinse <0.1µS • Spin drying	Only for Borofloat wafers! t = 2 minutes.
D	**Manually Aligning & Prebonding** (#bond001)	CR112B/Wet Bench • Contact wafers manually • Apply light pressure with tweezers • If necessary use tweezers to press out air-bubbles • Check prebonding by using IR-setup	
E	**Fusion bonding of Glass-Silicon, low-T** (#bond002)	TST: lab on 7th floor Furnace TOMA • Ramp-up: 1hr • Anneal time: 4hr at 400°C • Ramp-down: overnight	

A.2 Nano-ridge fabrication process

A.2.1 Mask layout and process outline

Mask layout

Only one mask is needed.
LINE: mask containing 4 μm lines and spacings



Process outline silicon wafer

Nr	Process steps	Cross-section after process
1 - 10	Substrate selection - Silicon <110> DSP Cleaning Standard Etching HF (1%) Native Oxide LPCVD SiRN - low stress LPCVD TEOS Lithography Olin907-12 (mask **LINE**)	
11 - 12	Etching HF 1% TEOS Stripping of Olin PR	
13 - 15	Standard Cleaning Etching SiRN (H_3PO_4) Stripping TEOS (1% HF)	
16 - 19	Silicon etching (OPD 4262) Standard Cleaning Etching HF (1%) Native Oxide Dry oxidation of silicon at 950°C (LOCOS)	
20 - 21	Etching SiRN (H_3PO_4) Silicon etching (OPD 4262)	

A.2.2 Silicon wafer processing

Nr	Process	Parameters	Remarks
1.	**Substrate selection Silicon <110> DSP** (#subs010)	CR112B / Wafer Storage Cupboard Orientation: <110> Diameter: 100mm ± mm Thickness: 380μm ± 10 μm Polished: Double side polished (DSP) Resistivity: 5-10Ωcm Type: p	Select <110> wafers.
2.	**Cleaning Standard** (#clean003)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
3.	**Etching HF (1%) Native Oxide** (#etch027)	CR112B / Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: >1min • Quick Dump Rinse <0.1μS • Spin drying	
4.	**LPCVD SiRN - low stress** (#depo002)	CR125C / Tempress LPCVD/HC Tube: G2 SiH_2Cl_2 flow: 70sccm NH_3 flow: 18sccm temperature: 850°C pressure: 200mTorr • program: SiRN deposition rate: 7.3 nm/min N_f: 2.14	Thickness 15 nm: 1 min deposition (start-up gives 8 nm already).
5.	**LPCVD TEOS** (#depo004)	CR112B / Tempress LPCVD Tube: B4-TEOS Bubbler: 40.0°C Temperature: 700°C pressure: 400mTorr • program: TEOS02 deposition rate: 7-13 nm/min	Thickness 40 nm: t=5 min.
6.	**Lithography - Priming (liquid)** (#lith001)	CR112B/Suss MicroTech Spinner (Delta20) Hotplate 120°C HexaMethylDiSilazane (HMDS) • Dehydration bake (120°C): 5min • Spinning acceleration: 4000rpm/s • Spinning speed: 4000rpm • Spinning time: 20s	

Nr	Process	Parameters	Remarks
7.	**Lithography - Coating Olin907-12** (#lith004)	CR112B/Suss MicroTech Spinner (Delta20) Hotplate 95°C Olin 907-12 • Spinning acceleration: 4000rpm/s • Spinning speed: 4000rpm • Spinning time: 20s • Prebake (95°C): 60s	
8.	**Lithography - Alignment & Exposure Olin 907-12 (EV)** (#lith020)	CR117B / EVG 20 Electronic Vision Group 20 Mask Aligner • Hg lamp: 12 mW/cm^2 • Exposure Time: 3.5 sec	
9.	**Lithography - Development Olin Resist** (#lith011)	CR112B / Wet-Bench 11 Developer: OPD 4262 Hotplate 120°C (CR112B or CR117B) • After Exposure Bake (120°C): 60sec Development: • Time: 30sec in Beaker 1 • Time: 15-30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	
10.	**Lithography - Postbake standard** (#lith009)	CR112B / Hotplate 120°C • Time: 30min	
11.	**Etching HF (1%) TEOS** (#etch027)	CR112B / Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 2.5 min • Quick Dump Rinse <0.1µS • Spin drying	Transfer of resist pattern to TEOS layer.
12.	**Stripping of Olin PR - standard** (#lith016)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 20min • Quick Dump Rinse <0.1µS • Spin drying • Visual microscopic inspection	
13.	**Cleaning Standard** (#clean003)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	

<table>
<tr><th>Nr</th><th>Process</th><th>Parameters</th><th>Remarks</th></tr>
<tr><td>14.</td><td>Etching of SiN
(Hot H_3PO_4)
(#etch053)</td><td>CR112B / Wet-Bench 3-1
H_3PO_4 85% Merck VLSI 1.00568.2500
Apply always first a Standard Wafer Clean and a ~~1% HF dip~~ to remove native oxide.
• Temp.: 180°C (caution!)
• Quick Dump Rinse <0.1µS
• Spin drying
Etchrate SiRN: 3.5 nm/min
High selective for SiO_2 layers
Only SiO_2, Silicon, PolySilicon, SiRN, SiON, SiON are allowed.
<table>
<tr><th>Temp. [°C]</th><th>etch rate Si_xN_y [nm/min]</th><th>etch rate (SiO_2) [nm/min]</th></tr>
<tr><td>180</td><td>4.1</td><td>0.48</td></tr>
<tr><td>160</td><td>1.4</td><td>0.16</td></tr>
<tr><td>140</td><td>0.5</td><td>0.05</td></tr>
</table></td><td>No 1% HF dip before etching!

Backside hydrophobic after rinsing with DI (cool wafer down gently before rinsing with DI).

Selectivity SiRN/SiO2: 9:1</td></tr>
<tr><td>15.</td><td>Etching HF (1%) Native Oxide
(#etch027)</td><td>CR112B / Wet-Bench 3-3
HF (1%) VLSI: MERCK 112629.500
• Etch time: 2.5 min
• Quick Dump Rinse <0.1µS
• Spin drying</td><td>TEOS stripping.</td></tr>
<tr><td>16.</td><td>Etching of Silicon by TMAH - ultra slow etch
(#etch049)</td><td>CR116B / Wet-Bench 2
Olin OPD 4262
A HF (1%) dip must have preceded this etching step
• Temp.: 25°C
• Quick Dump Rinse <0.1µS
• Spin drying
Etchrate (Si <110>) = 3.7nm/min</td><td><110> Si etch.

Etch time determines ridge height.</td></tr>
<tr><td>17.</td><td>Cleaning Standard
(#clean003)</td><td>CR112B / Wet-Bench 3-2
HNO_3 (100%) Selectipur: MERCK 100453
HNO_3 (69%) VLSI: MERCK 116445
• Beaker 1: fumic HNO_3 (100%), 5min
• Beaker 2: fumic HNO_3 (100%), 5min
• Quick Dump Rinse <0.1µS
• Beaker 3: boiling (95°C) HNO_3 (69%), 10min
• Quick Dump Rinse <0.1µS
• Spin drying</td><td></td></tr>
<tr><td>18.</td><td>Etching HF (1%) Native Oxide
(#etch027)</td><td>CR112B / Wet-Bench 3-3
HF (1%) VLSI: MERCK 112629.500
• Etch time: >1min
• Quick Dump Rinse <0.1µS
• Spin drying</td><td>1 min,
directly before
dry oxidation step.</td></tr>
</table>

<table>
<tr><th>Nr</th><th>Process</th><th>Parameters</th><th>Remarks</th></tr>
<tr><td>19.</td><td>Dry Oxidation (DOX) at 950°C of Silicon
(#depo031)</td><td>CR112B / Furnace A2
Standby temp.: 700°C
• Program: Dry-950
• Temp.: 950°C
• Gas: O_2
Growthrate:
<table>
<tr><th>Oxidation (min)</th><th>Si <100> oxide (nm)</th><th>Si <110> oxide (nm)</th></tr>
<tr><td>0</td><td>2.27</td><td>2.38</td></tr>
<tr><td>6</td><td>8.29</td><td>12.33</td></tr>
<tr><td>12</td><td>12.2</td><td>17.51</td></tr>
<tr><td>24</td><td>17.78</td><td>25.67</td></tr>
<tr><td>48</td><td>28.06</td><td>38.58</td></tr>
<tr><td>96</td><td>45.68</td><td>59.1</td></tr>
<tr><td>192</td><td>75.88</td><td>91.43</td></tr>
</table></td><td>LOCal Oxidation of Silicon.

Oxidation time determines ridge width.</td></tr>
<tr><td>20.</td><td>Etching of SiN (Hot H_3PO_4)
(#etch053)</td><td>CR112B / Wet-Bench 3-1
H_3PO_4 85% Merck VLSI 1.00568.2500
Apply always first a Standard Wafer Clean and a ~~1% HF dip~~ to remove native oxide.
• Temp.: 180°C (caution!)
• Quick Dump Rinse <0.1µS
• Spin drying
Etchrate SiRN: 3.5 nm/min
High selective for SiO_2 layers
Only SiO_2, Silicon, PolySilicon, SiRN, SiON, SiON are allowed.
<table>
<tr><th>Temp. [°C]</th><th>etch rate Si_xN_y [nm/min]</th><th>etch rate (SiO_2) [nm/min]</th></tr>
<tr><td>180</td><td>4.1</td><td>0.48</td></tr>
<tr><td>160</td><td>1.4</td><td>0.16</td></tr>
<tr><td>140</td><td>0.5</td><td>0.05</td></tr>
</table></td><td>SiN strip.

No 1% HF dip before etching!

Etch time from first SiN etch (step 14) (cool wafer down gently before rinsing with DI).</td></tr>
<tr><td>21.</td><td>Etching of Silicon by TMAH - ultra slow etch
(#etch049)</td><td>CR116B / Wet-Bench 2
Olin OPD 4262: XXXX
~~A HF (1%) dip must have preceded this etching step~~
• Temp.: 25°C
• Quick Dump Rinse <0.1µS
• Spin drying
Etchrate (Si <110>) = 3.7nm/min</td><td>Si <110> back-etch.

No 1% HF dip before etching!</td></tr>
</table>

A.3 LIL 2D nanochannel fabrication process

A.3.1 Mask layout and process outline

Mask layout

No mask is needed; the exposure is done using laser interference lithography.

Process outline silicon wafer

Nr	Process steps	Cross-section after process
1 - 4	Substrate selection - Silicon <110> DSP (with exaggerated native oxide layer) Standard Cleaning Resist coating	
5 - 7	LIL resist exposure and development (optionally image reversal procedure)	
8	1% HF/BHF pattern transfer to native oxide layer	
9	Resist stripping Wet anisotropic etching of silicon 1% HF oxide mask stripping	

A.3.2 Silicon wafer processing

Nr	Process	Parameters	Remarks
1.	**Substrate selection Silicon <110> DSP** (#subs010)	CR112B / Wafer Storage Cupboard Orientation: <110> Diameter: 100mm ± mm Thickness: 380µm ± 10 µm Polished: Double side polished (DSP) Resistivity: 5-10Ωcm Type: p	Si <110> wafer selection.
2.	**Cleaning Standard** (#clean003)	CR112B / Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 HNO_3 (69%) VLSI: MERCK 116445 • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1µS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1µS • Spin drying	
3.	**Lithography – Priming (gas phase)**	CR112B/HMDS Gas Phase Primer • Set oven to 150°C • Wafers in • Vacuum (1 bar - 26 inches Hg ≈ 0.1bar) • N_2 flush (decrease to 1 bar - 10 inches Hg) • Repeat the 2 former steps 3 times • Vacuum (1 bar - 26 inches Hg = 0.1bar) • Dehydration bake 30 min • V-HMDS 5 minutes • N_2 flush • Vacuum (1 bar - 26 inches Hg ≈ 0.1bar) • Repeat the 2 former steps 3 times • N_2 flush	
4.	**Lithography - Coating XXX.xxx (Headway)** Olin diluted TI 04XR Clariant AZ 1505	CR112B / Headway Spinner **Olin diluted** (EEP:MMP:OLIN 907-12/6:4:10) • Spinning speed: 3200 rpm • Spinning time: 30 s • Thickness: 0.4µm • Prebake (95°C): 5 min **TI 04XR** • Spinning speed: 4000 rpm • Spinning time: 20 s • Thickness: 0.4µm • Prebake (95°C): 1 min	Olin 907/12 resist has to be diluted prior to resist spinning.
5.	**Lithography - Alignment & Exposure**	**LIL** 150uw/cm^2 Exposure Time: • Olin diluted: 35 s • TI 04XR: 50 s • AZ 1505: 13-17 s	Laser interference lithography. Delay before further processing: at least 5 min.

Nr	Process	Parameters	Remarks
6.	**Image reversal bake (Only for TI-04)**	Hotplate • 4 minutes @ 130°C Flood exposure: • 12 seconds Karl Süss, 9mW/cm^2 Delay at least 5 minutes	Only for TI-04!
7.	**Lithography - Development**	CR112B / Wet-Bench 11 Developer: OPD 4262 Development: • Time: 30sec in Beaker 1 • Time: 30sec in Beaker 2 • Quick Dump Rinse <0.1µS • Spin drying	Use fresh developer solution.
8.	**Etching HF (1%) or BHF (7:1) Native oxide**	CR112B **HF (1%) VLSI: MERCK 112629.500** • Etch time: 1min • Etch rate: 5 nm/min • Water Rinse **BHF (1%)** • Etch time: 20 seconds • Etch rate: 5 nm/min • Water Rinse	Transfer of LIL resist pattern to native oxide layer.
9.	**Etching of Silicon by TMAH - ultra slow etch** (#etch049)	CR116B / Wet-Bench 2 Olin OPD 4262 A HF (1%) dip must have preceded this etching step • Temp.: 25°C • Quick Dump Rinse <0.1µS • Spin drying Etchrate (Si <110>) = 3.7nm/min	1min acetone 1min IPA OPD 4262 silicon etch (30 min) 1min HF mask strip QDR rinse Spin dry

Summary

This thesis deals with the fabrication and characterization of nanochannels (channels with at least one dimension in the sub-100 nm range). These channels are important for various areas of research, including DNA analysis systems and chemical sensors. In addition, the behavior of liquids in nano-confinement is of interest for many of the applications. The technologies currently used to fabricate nanochannels are often expensive and/or time consuming or simply not accurate enough. This creates a need for controlled, yet simple fabrication technologies.

Two possible methods were developed to fabricate nanochannels with a height below 100 nm. The first one is based on wet anisotropic etching of silicon, giving nanochannels with rectangular cross-sections. When extremely low depth of the channels is necessary (down to 5 nm), the use of a patterned silicon dioxide layer is advisable. Both technologies show excellent surface roughness and good uniformity. Sealing of the channels was achieved by direct bonding of the wafers to silicon or Borofloat glass wafers.
In addition, complete chips including nanochannels and integrated fluidic reservoirs, measurement rulers and power blasted access holes were designed and fabricated. The nanochannels on the chips have depths ranging from 5 to 150 nm.

To study the behavior of fluids in nano-confinement, the chips were filled with various liquids (water, sodium chloride solution and cyclohexane). The filling speed was compared to a theoretical model, based on Washburn's equation for capillary filling. Qualitative agreement with the model was confirmed, but quantitatively a reduced filling speed of the liquids was observed, the reduction becoming larger when the channel depth decreased.

In addition, two technologies were described to enable the fabrication of two-dimensional nanochannels, which have both a depth and a width in the nanometer range. Laser interference lithography, in combination with wet anisotropic etching of silicon is able to directly create such nanochannels. Local oxidation of silicon edges can provide very thin (sub-10 nm) nano-ridges, which can be transferred to a silicon wafer by imprint lithography.

In conclusion, the future fabrication of nanochannels can be greatly simplified when using the technology described in this thesis. Further research remains to be done on the characterization of fluid flow inside the channels.

Samenvatting

Dit proefschrift gaat over het fabriceren en karakteriseren van nanokanalen (kanalen waarvan tenminste één van de afmetingen kleiner is dan 100 nanometer). Dit soort kanalen is van belang voor een groot aantal toepassingen, waaronder DNA analyse en chemische sensoren. Daarnaast is het gedrag van vloeistoffen in deze kanalen interessant voor veel toepassingen. De technologieën die gebruikt worden voor de fabricage van nanokanalen zijn vaak duur en/of tijdrovend, of simpelweg niet nauwkeurig genoeg. Er is dus een noodzaak voor het ontwikkelen van methodes voor het gecontroleerd en eenvoudig fabriceren van deze kanalen.

Twee methodes zijn ontwikkeld voor het maken van nanokanalen met een diepte kleiner dan 100 nm. De eerste maakt gebruik van het nat anisotroop etsen van silicium, dit heeft nanokanalen met een rechthoekige doorsnede als resultaat. Als de diepte van de kanalen extreem klein moet zijn (tot 5 nm), kan het beste een laag siliciumdioxide gebruikt worden om de hoogte van het kanaal te definiëren. Beide technologieën leveren kanalen met zeer gladde oppervlakken en een lage spreiding in de kanaaldiepte. Het afdichten van de kanalen is bereikt door het bonden van de wafers met silicium of Borofloat glazen wafers.
Verder zijn chips gefabriceerd, compleet met nanokanalen, vloeistofreservoirs, meetstructuren en gepoederstraalde toegangsgaten. De nanokanalen hebben een diepte variërend van 5 tot 150 nm.

De chips zijn gevuld met vloeistoffen (water, natriumchlorideoplossing en cyclohexaan) teneinde het gedrag van vloeistoffen in de nanokanalen te bestuderen. Deze vulsnelheid van de kanalen is vergeleken met een theoretisch model, gebaseerd op de Washburn-vergelijking voor het vullen van kanalen door capillaire krachten. Kwalitatief is er goede overeenstemming met het model, maar naarmate

de kanaaldiepte afneemt wordt de kwantitatieve afwijking van de vulsnelheid ten opzichte van het model groter.

Ook zijn twee fabricagemethodes voor tweedimensionale nanokanalen (met breedte én diepte in de ordegrootte van nanometers) ontwikkeld. De eerste combineert laser interferentie lithografie met nat etsen van silicium. Met behulp van de tweede methode kunnen zeer dunne nano-richeltjes gemaakt worden door silicium lokaal te oxideren. Deze kunnen vervolgens door middel van imprint lithografie overgebracht worden op een andere wafer.

Concluderend kan worden gesteld dat de fabricage van nanokanalen aanzienlijk vereenvoudigd kan worden met behulp van de resultaten van dit onderzoek. Verder onderzoek naar het gedrag van vloeistoffen in de kanalen is wenselijk.

Dankwoord

Het leukste stukje om te lezen is volgens goed gebruik tot het laatst bewaard… Iedereen die me op enig moment geholpen heeft, meegedacht heeft, raad heeft gegeven, opgevrolijkt heeft, gekalmeerd heeft, me op mijn fouten gewezen heeft (er waren er genoeg): bedankt! Maar omdat dit wel erg kortaf zou zijn, wil ik deze gelegenheid graag aangrijpen om een aantal van jullie persoonlijk te bedanken.

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Het aandeel van de MicMec technologen Meint (kun je nog van Bassie winnen met fietsen?), Erwin (J: "Erwin, het is compleet mis gegaan in de clean room!" E: "O ja, laat 's zien? Hmm, misschien kúnnen we daar wel wat mee…") en Rik mag niet worden onderschat. Zonder jullie lag de vakgroep op z'n kont. Dan kom ik uit bij Pino: samen iets meten hoefden we nooit, maar de kerstboom opzetten is eigenlijk ook veel leuker. Bedankt voor al het plezier dat we samen hebben gehad!

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Een zoen van Jeroen

P.S. Omdat ze dan toch ergens vastgelegd zijn, én omdat het zo'n fantastische uitspraak is, nog eenmaal de woorden van mijn oma nadat ik haar vertelde dat ik Technische Natuurkunde ging studeren: "O, iets met de natuur is altied mooi." Oma, bedankt!